

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte BALAMURUGAN SUBRAMANIAN

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Appeal No. 2004-1834  
Application No. 10/158,885

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ON BRIEF

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Before THOMAS, KRASS, and JERRY SMITH, Administrative Patent Judges.  
KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1-14.

The invention pertains to the area of wafer processing. In particular, the invention is a method of processing partial wafers of random sizes in pick and place equipment, and seeks to improve upon the prior art methods wherein locator dies are required or the last column of the first row contains a die.

Representative independent claim 1 is reproduced as follows:

1. A method of processing partial wafers comprising the step of:

making all partial wafer cuts perpendicular to the wafer flat with all partial wafer cuts following a cut sequence where the first cut section is with a reference die and the other cut sections are in the numerical order from right to left with the first partial wafer of the full wafer having a reference die;

identifying a pseudo reference die for each partial wafer not having a reference die which die is the first die in the bottom right;

moving wafer table to the last left column of the partial wafer and determining the coordinate;

storing the coordinate of the last left column in a wafer map data file;

removing all dies from the wafer map that are not part of the partial wafer using said coordinate; and

performing picking and placing dies.

The examiner relies on the following reference:

Balamurugan	6,174,788	Jan. 16, 2001
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The examiner also relies on admitted prior art (APA) described at paragraph 3 of the instant specification.

Claims 1-14 stand rejected under 35 U.S.C. §103. As evidence of obviousness, the examiner offers Balamurugan with regard to claims 1-4, and 6-11, adding APA with regard to claims 5, and 12-14.

Reference is made to the briefs and answer for the respective positions of

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appellant and the examiner.

### OPINION

It is the examiner's position that, with regard to independent claims 1 and 8-11, Balamurugan discloses the claimed subject matter but for "the language of moving wafer table to the last left column and the label of the coordinates being identical to the instant application" (answer-page 3).

In particular, the examiner points to column 4, lines 57-58, for making all partial cuts perpendicular to the wafer flat; to column 4, line 59, for a teaching of all partial cuts following a cut sequence where the first cut section is with a reference die; to column 4, lines 62-64, for other cut sections are in numerical order from right to left; and to column 4, line 59, for a teaching of the first partial wafer of the full wafer having a reference die.

The examiner contends that Balamurugan identifies a pseudo reference die for each partial wafer not having a reference die in which the die is the first die in the bottom right (citing the auxiliary reference die in Figure 4), since this auxiliary reference die meets appellant's definition, at page 10 of the specification, as a die that acts as a reference die if there is no reference die available.

The examiner contends, further, that Balamurugan moves the wafer table to the last die in the row of the partial wafer and determines the coordinates, at column 5, lines 14-20.

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It is the examiner's contention that although not stated in like language, "the die referred to in the instant application (figure 9, last column of a partial) and in Balamurugan (figure 22, auxiliary reference die) are identical. Balamurugan removes all dies from the wafer map that are not part of the partial wafer using said coordinate (column 5 lines 19 and 26-28), and picks and places dies (removing is picking, column 1 lines 29-30, the good dies are picked up and placed)" (answer-page 4).

In a similar manner, the examiner has identified corresponding portions of Balamurugan with regard to the elements of instant claims 2-4 and 6-11, at pages 4-6 of the answer, and concludes that it "would be [have been] obvious...to modify Balamurugan to include moving from one column to another as moving to the left as shown by figure 15 and to label the auxiliary die x1,y1 rather than the locator [sic, locator] die labeled x1,y1 as the labeling is not critical to the wafer movement" (answer-pages 6-7).

The examiner does appear to have set forth a prima facie case of obviousness by citing art which establishes the level of skilled artisans, by pointing out the elements of the reference which correspond to the elements of the instant claims, and by giving

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reasons why it would have been obvious to the artisan to modify the prior art in order to arrive at the instant claimed subject matter.

Therefore, the burden has shifted to appellant to rebut this prima facie case of obviousness, either by objective evidence or convincing argument.

Appellant sets forth general arguments as to how the instant invention is an improvement over Balamurugan in that the reference requires a locator die coordinate and uses the wafer map host to store and manipulate the data (e.g., see pages 9-11 of the principal brief). Appellant also explains how the definitions of a “pseudo reference die” and an “auxiliary reference die” differ.

These arguments by appellant, even if accurate, are directed to possible differences between Balamurugan and the instant *disclosed* invention. Since appellant fails to point to any distinguishing *claim* language, these arguments are not persuasive of nonobviousness.

At page 11 of the principal brief, appellant refers to specific claim language in contending that Balamurugan fails to suggest using a coordinate, determined after moving the wafer table to the last left column of the partial wafer, to remove all dies that are not part of the partial wafer. Moreover, appellant argues that Balamurugan fails to suggest “storing the coordinate of the last left column.

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The examiner identifies Figure 15 and column 5, lines 14-20, of Balamurugan for movement of the wafer table to the locator die and determining coordinates. The examiner also identifies column 5, lines 26-28, of Balamurugan, for the removal of all dies from the wafer map that are not part of the partial wafer using the coordinates determined after wafer table movement.

These portions of Balamurugan identified by the examiner do, indeed, seem to disclose the features appellant argues are not suggested by Balamurugan.

In reply, appellant again argues the problems of Balamurugan which are overcome by the instant invention by processing partial wafers even if the last column of the first row does not contain a die and without both x and y coordinate information and without a reference die (reply brief-page 4). While this may be true, appellant points to no specific claim language which distinguishes over the prior art in this manner.

Appellant further argues that, in Balamurugan, the last partial wafer must contain at least one full die in the reference die row and that this "is not a requirement of the present invention." While this may not be a requirement of the present invention, the instant claimed invention also does not preclude the possibility of the last partial wafer containing at least one full die in the reference die row. Therefore, this argument is not persuasive of nonobviousness.

Specifically, appellant argues that Balamurugan allows the local fab to find the dies to be picked using a wafer map “without the many steps” of Balamurugan “to determine using a whole wafer map where the locator die is” (reply brief-page 4). The language of claim 1 relied on is “identifying a pseudo reference die for each partial wafer not having a reference die which die is the first die in the bottom right.” Appellant contends that in the reference the auxiliary reference die row is always in the reference die row (column 5, lines 36-37), which requires information on where the reference die is. Thus, according to appellant, in Balamurugan, if there is no reference die and the location of the reference die is not known, Balamurugan’s method cannot determine where the auxiliary die is located. The present invention does not have to know where the reference die is located because it uses the pseudo reference die which is the first die on the bottom right or the next die column number after the last column number of the previous partial wafer.

Notwithstanding arguments that may be directed to the instant *disclosed* invention, Appellant is arguing the claim 1 language, “identifying a pseudo reference die for each partial wafer not having a reference die which die is the first die in the bottom right.” But Balamurugan clearly states that a “reference die is located in the first partial wafer P1 and an auxiliary reference die is located in other partial wafers P2 to P5 in the lower right corner on the same row as the reference die” (column 4, lines

38-41). With the examiner equating Balamurugan's "auxiliary reference die" to appellant's claimed "pseudo reference die," this disclosure of Balamurugan appears to us to disclose exactly what is claimed. Accordingly, we do not find appellant's argument to be persuasive.

At page 5 of the reply brief, appellant explains that the left column coordinate in the present application need not be in the reference die row, which is a requirement of Balamurugan for the locator die. Thus, appellant concludes that there is no suggestion of storing this last column value which is used for the subsequent partial wafers in the same wafer map and nothing in the reference suggests using such a coordinate to remove all dies as not part of the partial wafer. Appellant contends that Balamurugan "teaches away" from the present invention because the reference is "dependent on the procedures discussed in [Balamurugan] to determine the auxiliary reference and locator die coordinates and a full die in the reference die row" (reply brief-page 5).

With regard to the "storing the coordinate of the last left column in a wafer map data file" of claim 1, appellant argues that this is not taught by Balamurugan because appellant's process permits processing at other fab locations with less data. Appellant points to instant Figure 26 for an explanation of the differences between the prior art and the instant invention (see page 6 of the reply brief). Appellant also makes other arguments regarding perceived examiner's error in equating a last left column with a

locator die and in equating a wafer map host with a wafer map data file, arguing that a wafer map host also manipulates data, which a file does not do.

The problem with appellant's arguments, as we see it, is that there are many arguments with regard to the present invention differing from that disclosed by Balamurugan, but there are few arguments pointing to specific claim language. Accordingly, it is unclear in many of the arguments as to just what claim language appellant relies on to distinguish the instant *claimed* invention from the disclosure of Balamurugan. Then in those arguments specifically pointing to claim language, appellant argues that Balamurugan does not disclose or suggest the cited claim language but appellant never convincingly rebuts the examiner's specific identification, in Balamurugan, of the claimed features. That is, while appellant argues that the reference does not show or suggest a particular claimed feature, appellant has not shown, convincingly, any error in the examiner's reasoning. For example, appellant contends that a file is not a wafer map host with manipulation. Yet, claim 1 says nothing about any "manipulation." It calls for a "wafer map data file" and the examiner has pointed to column 5, lines 63-64, of Balamurugan for a showing of a "wafermap data host" to which locator die coordinates are uploaded. Accordingly, it seems that, in Balamurugan, coordinates are stored in a wafermap data host and must therefore be stored in some type of "file." If the file is in a "wafermap data host," it appears that the

coordinates are stored in a wafer map data file, as broadly claimed. As another example, appellant makes much of the claimed step of “moving wafer table to the last left column of the partial wafer and determining the coordinates” by arguing that the reference does not suggest this. However, the examiner very reasonably points to Figure 15, and column 5, lines 14-20, of Balamurugan, wherein Figure 15 shows movement to the last left column of the partial wafer, and column 5, lines 14-20, clearly point to determining coordinates, as broadly claimed. For all of appellant’s posturing about the differences between the “new method” of the instant invention and the prior art, as depicted by Balamurugan, appellant has not convinced us of any error in the examiner’s rationale regarding the broad recitations of the instant claims.

Accordingly, we will sustain the rejection of claim 1 under 35 U.S.C. §103.

With regard to claim 2, appellant argues that the “last column in the present application is not dependent on their (sic, there) being a reference die or any die in the reference die row and in some cases does not have to be searched for but given in the header” (principal brief-pages 11-12). Again, appellant argues generalities as to the instant *disclosed* invention, without pointing to any specific claim language upon which he relies for patentability. Accordingly, and in view of the examiner’s reasonable explanation as to how Balamurugan is applied to the claim, we will sustain the examiner’s rejection of claim 2 under 35 U.S.C. §103.

As to claim 3, appellant argues that Balamurugan fails to mention a last column number or of placing this last column number in the header of the wafer map data file for the next partial wafer. The examiner does not deny that Balamurugan fails to teach a header. However, the rejection is under 35 U.S.C. §103 and the examiner finds that the wafer map host of the reference includes data for the last column number and that as data from each partial wafer is uploaded into the wafer map, the same wafer map data file is used for all partial wafers with different last column values (pointing to column 5, lines 60-64, and column 6, lines 2-7). The examiner also admits that Balamurugan may not specifically teach how an information file is organized (answer-page 14), though the examiner finds that the wafer map host of Balamurugan includes data for the last column number. Since appellant appears to admit that Balamurugan provides a map for the whole wafer, the examiner contends that this suggests that the map data host is a singular file with sub files for each partial wafer. Since data is uploaded into the file and retrieved for the next cut, the examiner contends that “how the files are titled (header) does not affect the process” and that “[a]s the cut depends upon the location of that column, the information is within the file, if not in a header” (answer-page 14). Accordingly, the examiner contends that it would have been obvious to provide the last column number in a header in Balamurugan. We find the

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examiner's reasoning to be sound and that appellant has not convinced us of an error in the examiner's rationale, even though Balamurugan does not specifically identify a "header," as claimed. Thus, we will sustain the examiner's rejection of claim 3 under 35 U.S.C. §103.

As to claim 4, appellant argues that no last column information of any kind is found in Balamurugan and, therefore, the reference cannot suggest the storage of last column information in a wafer map data file. We find the examiner's rationale to be reasonable, in finding that the listing, by Balamurugan, of locator dies, uses the last column information (pointing to Figure 22) and continuously updates information, in steps 16 and 23, and uses this map file for all partial wafers. Appellant has not convinced us of any error in the examiner's findings. Therefore, we will sustain the rejection of claim 4 under 35 U.S.C. §103.

In claim 6, the last column and wafer identification are stored in a separate file not associated with a wafer map data file and the last column information is retrieved from storage before processing a partial wafer. Appellant contends that this is not taught by Balamurugan. The examiner contends that the data of the partial wafer is stored in a file and that this is a "separate file," as broadly claimed.

We will sustain the rejection of claim 6 because the examiner's explanation, at pages 15-16 of the answer, as to why the storing of partial wafer data in a file suggests

storing this data in a “separate file” appears reasonable. In responding to appellant’s argument, the examiner questions the “not associated” language of the claim. In particular, at page 15 of the answer, the examiner contends that the base claim limits the information as to the last column to be stored in a wafer map data file, and that information placed in a wafer map data file can be placed in a separate (a second or back up) file, but having the same information, it cannot be “not associated” with the wafer map data file. The examiner appears to be questioning the definiteness of the claim language but, more importantly, it appears that the examiner is contending that the reference teaches a “separate file not associated with a wafer map data file” at least to the same extent as such a feature is claimed and disclosed by appellant. Since appellant has not offered anything that convinces us of any error in this position of the examiner, we will sustain the rejection of claim 6 under 35 U.S.C. §103.

With regard to claim 7, the examiner explains the rejection by contending that data of a partial wafer is used to pick and place dies and, at the time of picking and placing, only data that pertains to the partial wafer is available; and that as this data is available for picking and placing, this partial wafer data map is available prior to the step of picking and placing. Thus, there is pre-processing, as claimed. Appellant’s only response is to state that the reference does not disclose this claimed step. This is

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not a convincing argument in view of the examiner's explanation. As appellant shows no error in the examiner's rationale. Thus, we will sustain the rejection of claim 7 under 35 U.S.C. §103.

With regard to claim 8, the examiner agrees with appellant that Balamurugan does not specifically teach a header. However, the rejection is under 35 U.S.C. §103 and the examiner provides a reason as to why it would have been obvious to provide the information called for in claim 8, i.e., that each file or subfile must have a form of identification in it and steps 22 and 23 of Balamurugan obtain and upload the locator coordinates (i.e., starting column), so that the same information is within the file (answer-page 16). In view of this reasoning, appellant does not point to an error in the examiner's rationale but, rather, merely contends that the reference does not teach a header, as claimed. Accordingly, we find for the examiner as to claim 8 and will sustain the rejection of this claim under 35 U.S.C. §103.

We also will sustain the rejection of claims 9-11 under 35 U.S.C. §103. As to these claims, appellant again merely sets forth recitations of the claims (pages 13-14 of the principal brief) without pointing out the alleged errors in the examiner's reasoning. When viewed in light of the examiner's rationale, at pages 3-4 and 16-17 of the answer, we find for the examiner.

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As to the rejection of claims 5, and 12-14, the examiner relies on APA for the limitations regarding assigning a bin number and placing picked dies in the die bin, and finds that it would have been obvious to modify Balamurugan by including bin numbers in the wafer map and to place dies into assigned bin numbers as a method of wafer mapping to keep track of dies (answer-page 7).

While appellant argues these claims, at pages 14-15 of the principal brief, the arguments are, for the most part, repetitious of previous arguments addressed supra. Moreover, appellant does not seem to even address APA upon which the examiner relies to make the combination. Accordingly, we will sustain the rejection of claims 5 and 12-14 under 35 U.S.C. §103.

We have sustained the rejection of claims 1-14 under 35 U.S.C. §103. Accordingly, the examiner's decision is affirmed.

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No time period for taking any subsequent action in connection with this appeal  
may be extended under 37 CFR § 1.136(a) (1) (iv).

AFFIRMED

JAMES D. THOMAS	)	
Administrative Patent Judge	)	
	)	
	)	
	)	
	)	BOARD OF PATENT
ERROL A. KRASS	)	APPEALS
Administrative Patent Judge	)	AND
	)	INTERFERENCES
	)	
	)	
JERRY SMITH	)	
Administrative Patent Judge	)	

EAK/vsh

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TEXAS INSTRUMENTS INCORPORATED  
P.O. BOX 655474, M/S 3999  
DALLAS, TX 75265