

The opinion in support of the decision being entered today was **not** written for publication and is **not** binding precedent of the Board.

Paper No. 25

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SEUNGMOO CHOI, SAILESH MERCHANT
and PRADIP K. ROY

Appeal No. 2004-2095
Application No. 09/384,503

ON BRIEF

Before PAK, WALTZ, and PAWLIKOWSKI, Administrative Patent Judges.
PAK, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on an appeal from the examiner's refusal to allow claims 15 and 17 through 21. Claims 1 through 14, the remaining claims in this application, stand withdrawn from consideration by the examiner as being directed to a non-elected invention.

The subject matter on appeal is directed to a method of fabricating "an integrated circuit having a DRAM with an ultra thin active layer formed on a SOI layer in which a low I_{off} can be

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achieved." See the specification, page 5, lines 20-22. Details of this appealed subject matter are recited in claim 15 which is reproduced below:

15. A method of fabricating an integrated circuit located on a semiconductor wafer, comprising:

forming a doped base substrate;

forming an insulator layer on the doped base substrate; and

forming a doped ultra thin active layer on the insulator layer to a thickness ranging from about 10nm to about 15 nm, the ultra thin active layer including a gate oxide, a gate formed on the gate oxide wherein a width of the gate oxide is coextensive with a width of the gate; and source and drain regions formed in the ultra thin active layer and adjacent the gate.

In support of his rejections, the examiner relies on the following prior art references:

Yoshimi et al. (Yoshimi)	5,698,869	Dec. 16, 1997
Yamazaki et al. (Yamazaki)	6,323,072 B1	Nov. 27, 2001

The appellants' admission at page 9 of the specification referring to prior art Figure 1 in the application (hereinafter referred to as "admitted prior art").

The appealed claims stand rejected as follows:

- (1) Claims 15, 17 through 19 and 21 under 35 U.S.C. § 103 as unpatentable over the combined teachings of the admitted prior art and Yamazaki; and
- (2) Claim 20 under 35 U.S.C. § 103 as unpatentable over the combined teachings of the admitted prior art, Yamazaki and Yoshimi.

We reverse.

The claimed method of fabricating an integrated circuit on a semiconductor wafer as represented by claim 15 is admittedly known, except for forming a doped ultra thin active layer having a thickness ranging from about 10nm to about 15 nm on an insulator layer. See the specification, pages 5 and 9. The admittedly known method is directed to forming an active layer having a thickness "typically [ranging] from about 600 nm to about 800 nm..." See the specification, page 5.

To remedy this deficiency in the admittedly known integrated circuit fabricating method, the examiner relies on the disclosure of Yamazaki. See the Answer, pages 3-5. Yamazaki recommends employing an active layer having a thickness falling "within a range of from 20 to 30 nm, preferably at 24 nm" to reduce the tune-off current in magnitude. See column 24, lines 52-57. However, as correctly pointed out by the appellants (the Brief, page 7), this active layer does not have a thickness which is inclusive of the claimed thickness. *Compare In re Sebek*, 465 F.2d 904, 907, 175 USPQ 93, 95 (CCPA 1972) ("Where, as here, the prior art disclosure suggests the outer limits of the range of suitable values, and that the optimum resides within that range, and where there are indications elsewhere that in fact the optimum should be sought

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within that range, the determination of optimum values outside that range may not be obvious."). More importantly, this active layer is said to be useful only in a case where a thermal oxide film of 20 nm is formed at the interface between the active layer and silicon oxide layer and where a width of a gate oxide is not coextensive with a width of a gate as urged by the appellants. See Yamazaki, column 24, lines 52-55 and Figures 4A-4E, together with the Brief, pages 8-11 and the Reply Brief, page 3.

The examiner also relies on the disclosure of Yoshimi. See the Answer, page 6. However, it is relied upon to show that it is well known to employ an insulating layer having the claimed thickness. See the Answer, page 6. The examiner does not refer to any teaching in Yoshimi to remedy the above deficiency. See the Answer in its entirety.

Thus, we are constrained to agree with the appellants that the applied prior art references as whole would not have led one of ordinary skill in the art to form an active layer having the claimed thickness during the admittedly known integrated circuit fabrication method. Specifically, the examiner, on this record, has not proffered sufficient evidence to demonstrate that the claimed ultra thin active layer is useful for the known DRAM device of the type discussed in the specification.

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In view of the foregoing, we reverse the examiner's decision
rejecting all of the claims on appeal under 35 U.S.C. § 103

REVERSED

CHUNG K. PAK)	
Administrative Patent Judge)	
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)	
)	
)	BOARD OF PATENT
THOMAS A. WALTZ)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
)	
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)	
BEVERLY A. PAWLIKOWSKI)	
Administrative Patent Judge)	

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