

The opinion in support of the decision being entered today was not written for publication in a law journal and is not binding precedent of the Board.

Paper No. 29

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MAHJOUB ALI ABDELGADIR and ALVARO MAURY

Appeal No. 2005-0339
Application No. 09/376,039

ON BRIEF

Before KIMLIN, PAK and TIMM, Administrative Patent Judges.

KIMLIN, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1, 2, 4-19 and 21-28, all the claims remaining in the present application. Claim 1 is illustrative:

1. A method of making an integrated circuit comprising:

forming a conductive layer, having conductive lines with gaps therebetween, adjacent a semiconductor substrate, including forming at least some of the conductive lines with different widths;

depositing a fluoro-silicate glass (FSG) layer including forming peaks having larger heights for larger widths of the conductive lines, by high-density plasma chemical vapor

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deposition (HDP-CVD), over the patterned conductive layer and to fill the gaps between conductive lines;

leaving the deposited FSG layer exposed;

chemically mechanically polishing the exposed FSG layer to reduce the height of the peaks to a substantially uniform height; and

depositing an undoped oxide layer on the exposed FSG layer after the chemical mechanical polishing of the FSG layer.

The examiner relies upon the following references as evidence of obviousness:

Lee	6,008,120	Dec. 28, 1999
Usami et al. (Usami)	6,157,083	Dec. 5, 2000

Appellants' claimed invention is directed to a method of making an integrated circuit by depositing a fluoro-silicate glass (FSG) layer over a patterned conductive layer on a semiconductor substrate. The FSG layer fills the gaps between the conductive lines and also forms peaks of non-uniform height over the conductive lines. The FSG layer is chemically mechanically polished to reduce the height of the peaks to a uniform height, and then an undoped oxide layer is deposited on the exposed FSG layer.

Appealed claims 1, 2, 4-19 and 21-28 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee in view of Usami.

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Appellants submit at page 7 of the principal brief that "[c]laims 1, 2, 4-19 and 21-28 stand or fall together." Accordingly, all the appealed claims stand or fall together with claim 1.

We have thoroughly reviewed each of appellants' arguments for patentability. However, we are in complete agreement with the examiner that the claimed method would have been obvious to one of ordinary skill in the art within the meaning of § 103 in view of the applied prior art. Accordingly, we will sustain the examiner's rejection for essentially those reasons expressed in the Answer.

Lee, like appellants, discloses a method of making an integrated circuit comprising the claimed steps of forming a conductive layer having conductive lines with gaps therebetween on a semiconductor substrate, depositing an FSG layer in the gaps and over the conductive layer to form peaks of non-uniform height, and depositing an undoped oxide layer on the FSG layer. Lee does not teach polishing the FSG layer before depositing the undoped oxide layer thereon. However, Usami teaches filling the spaces between the conductive lines on a substrate with FSG layers and polishing the second FSG layer to produce peaks of uniform height before coating the undoped oxide layer on the

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planarized FSG layer. Also, as noted by the examiner, Usami teaches that it was known in the prior art to polish and planarize an FSG layer before performing further operations in making an integrated circuit. Accordingly, we are satisfied that it would have been obvious for one of ordinary skill in the art to planarize the FSG layer of Lee with chemical mechanical polishing before applying the undoped oxide coating. Although Usami provides two FSG layers of different composition before planarizing the top layer, and the presently claimed method deposits only a single FSG layer, we find that one of ordinary skill in the art would have found it obvious to eliminate one of the FSG layers of Usami along with its attendant advantage. See In re Thompson, 545 F.2d 1290, 1294, 192 USPQ 275, 277 (CCPA 1976); In re Kuhle, 526 F.2d 553, 555, 188 USPQ 7, 9 (CCPA 1975); In re Edge, 359 F.2d 896, 899, 149 USPQ 556, 557 (CCPA 1966).

Appellants contend that the prior art discussed by Usami does not teach or suggest the claimed invention "since the peaks of the FSG layer 302 illustrated therein are also completely polished away, rather than polished to reduce the height of peaks to a substantially uniform level" (sentence bridging pages 12 and 13 of principal brief). However, since appellants acknowledge that "those who are skilled in the art understand that fully

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planarizing a surface is far more difficult, time consuming and expensive than performing CMP to simply reduce the height of peaks to a substantially uniform level" (page 13 of principal brief, first full sentence), we find that one of ordinary skill in the art would have found it obvious to avoid polishing the FSG layer all the way down to the conductive layer in order to save the known added cost. We are confident that it would have been within the skill of one of ordinary skill in the art to resort to a cost/benefit analysis in determining how much of the FSG layer to remove during the polishing operation. Moreover, we agree with the examiner that the claims on appeal do not preclude the complete planarization of the peaks to the height of the conductive layer. The claim language "to reduce the height of the peaks to a substantially uniform height" includes reducing the height of the peaks to zero.

While we agree with appellants that it is not proper for the examiner to consider FSG layers 203 and 204 of Usami as a single FSG layer, we nevertheless conclude, for the reasons expressed above, that the claimed method would have been obvious to one of ordinary skill in the art.

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As a final point, we note that appellants base no argument upon objective evidence of nonobviousness, such as unexpected results.

In conclusion, based on the foregoing, the examiner's decision rejecting the appealed claims is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a)(1)(iv) (effective Sep. 13, 2004; 69 Fed. Reg. 49960 (Aug. 12, 2004); 1286 Off. Gaz. Pat. Office 21 (Sep. 7, 2004)).

AFFIRMED

EDWARD C. KIMLIN)	
Administrative Patent Judge)	
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CHUNG K. PAK)	BOARD OF PATENT
Administrative Patent Judge)	APPEALS AND
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