

The opinion in support of the decision being entered today was *not* written for publication and is *not* binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MARK L. JANECEK, JOHN S. KRESGE,
MARK V. PIERSON, and THURSTON B. YOUNGS, JR.

Appeal No. 2005-0624
Application No. 09/853,506

ON BRIEF

Before JERRY SMITH, OWENS, and NAPPI, *Administrative Patent Judges*.

OWENS, *Administrative Patent Judge*.

DECISION ON APPEAL

This appeal is from a rejection of claims 1, 2, 4-7, 11, 12 and 14.

THE INVENTION

The appellants claim a laminated circuit structure and a method for making it. Claim 1, which claims the structure, is illustrative:

1. A three-layered, laminated circuit structure, comprising:

a first substrate having conductive via through holes disposed therein;

a second substrate laminated to said first substrate and having conductive, adhesive-filled via through holes that align with, and make electrical contact with, the conductive via through holes of said first substrate; and

a third substrate laminated to said second substrate having via through holes that align with, and make electrical contact with, the adhesive filled via through holes of said second substrate, thus forming said three-layered, laminated circuit structure.

THE REFERENCE

DiStefano et al. (DiStefano) 5,640,761 Jun. 24, 1997

THE REJECTION

Claims 1, 2, 4-7, 11, 12 and 14 stand rejected under 35 U.S.C. § 102(b) as being anticipated by DiStefano.

OPINION

We affirm the aforementioned rejection.

The appellants indicate that the claims stand or fall together (brief, page 4).¹ We therefore limit our discussion to

¹ To the extent that the appellants' argument that claim 5 requires slightly undercut conductive pads that are not disclosed by DiStefano is a separate argument for patentability (brief, page 6), this argument is not well taken because the appellants are arguing a limitation that is not in claim 5. See *In re Self*, 671 F.2d 1344, 1348, 213 USPQ 1, 5 (CCPA 1982).

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one claim, i.e., claim 1. See *In re Ochiai*, 71 F.3d 1565, 1566 n.2, 37 USPQ2d 1127, 1129 n.2 (Fed. Cir. 1995); 37 CFR § 1.192(c)(7)(1997).

DiStefano discloses a three-layered laminated circuit structure comprising circuit panel 10a having conductive via through holes 26 disposed therein, an interposer layer 12a laminated to circuit panel 10a and having conductive, adhesive-filled via through holes 48 that align with, and make electrical contact with, the conductive via through holes of circuit panel 10a (col. 4, lines 57-59; col. 16, line 52 - col. 17, line 19; col. 18, lines 40-43; col. 19, lines 3-9, 17-31, 38-47 and 63-66), and a circuit panel 10b which is laminated to interposer layer 12a and has via through holes that align with, and make electrical contact with, the adhesive filled via through holes of interposer layer 12a (col. 18, lines 43-47; figure 2).

The appellants argue that DiStefano's interposer layer 12a is not designed as a power core layer (brief, page 5). This argument is not convincing because it is directed toward a limitation which is not in claim 1. See *In re Self*, 671 F.2d 1344, 1348, 213 USPQ 1, 5 (CCPA 1982).

The appellants argue that DiStefano's interposer layer 12a does not have a distinct plated via through hole that aligns with plated via through holes of circuit panels 10a and 10b (brief, page 5). The appellants are incorrect. DiStefano's interconnect location 46a of via 48a in interposer layer 12a is aligned with interconnect location 56a of via 26 in circuit panel 10a, and interconnect location 47a opposite interconnect location 46a in interposer layer 12a is aligned with interconnect location 58a of via 26 in circuit panel 10b (col. 18, lines 40-47).

The appellants argue that "because [DiStefano's] dielectric elements 38 and 40 are flowable, it is not possible that the interposer layer can properly be described as making the alignment of the vias by way of lamination" (brief, page 6). This argument is not well taken because DiStefano teaches that "[t]he flowable dielectric material layers **38** and **40** are interrupted by the holes and by elements **48** so that the flowable conductive [sic, dielectric] material is not present at interconnect locations **46** and **47** of the interposer" (col. 16, lines 48-51). Although some dielectric material of layers 38 and 40 can bulge into space originally occupied by flowable conductive material 48a in a via of the interposer layer (col. 20, lines 55-58), the conductive material 48a still is

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aligned and makes electric contact with conductive material 26a in a via of circuit panel 10a and conductive material 26b in a via of circuit panel 10b (figure 3).

We therefore find that the circuit structure claimed in the appellants' claim 1 is anticipated by DiStefano. Accordingly, we affirm the rejection of that claim and claims 2, 4-7, 11, 12 and 14 that stand or fall therewith.

DECISION

The rejection of claims 1, 2, 4-7, 11, 12 and 14 under 35 U.S.C. § 102(b) over DiStefano is affirmed.

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No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a)(1)(iv)(effective September 13, 2004; 69 Fed. Reg. 49960 (August 12, 2004); 1286 Off. Gaz. Pat. and TM Office 21 (September 7, 2004)).

AFFIRMED

JERRY SMITH)	
Administrative Patent Judge)	
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TERRY J. OWENS)	BOARD OF PATENT
Administrative Patent Judge)	APPEALS AND
)	INTERFERENCES
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ROBERT E. NAPPI)	
Administrative Patent Judge)	

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MARK LEVY
SALZMAN & LEVY
19 CHENANGO ST., STE. 902
BINGHAMTON, NY 13901