

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte PHILIP C. BARNETT and DAVID SOWARDS

Appeal No. 2005-1295
Application No. 10/376,682

ON BRIEF

Before THOMAS, KRASS, and BLANKENSHIP, Administrative Patent Judges.
BLANKENSHIP, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1-6 and 8-14.

We affirm-in-part.

BACKGROUND

The invention is directed to a single chip embedded microcontroller (e.g., for use in a smart card) that may communicate with PROM arrays consisting of an OTPROM (one time programmable read only memory) and an EEPROM (electrically erasable programmable read only memory). Representative claim 1 is reproduced below.

1. A single chip embedded microcontroller comprising,
 - a processor,
 - a first non-volatile erasable PROM array having a communication link with said processor, said processor capable of reading, erasing and writing information to and from said first non-volatile erasable PROM, wherein said erasing of said first non-volatile erasable PROM array is performed on a plurality of bytes,
 - a second non-volatile erasable PROM array having a communication link with said processor, said processor capable of reading, erasing and writing information to and from said second non-volatile erasable PROM, wherein said erasing of said second non-volatile erasable PROM array is performed on a single byte,
 - a high voltage generator having a communication link with said processor, said high voltage generator generating two or more different erase and write voltages, and
 - a switch communicating with said high voltage generator, said switch connects said two or more different erase and write voltages between said first and second non-volatile erasable PROM arrays.

The examiner relies on the following references:

Koizumi	5,504,707	Apr. 2, 1996
Talreja	5,742,787	Apr. 21, 1998

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Claims 1-5 and 8-13 stand rejected under 35 U.S.C. § 102 as being anticipated by Koizumi.

Claims 6 and 14 stand rejected under 35 U.S.C. § 103 as being unpatentable over Koizumi and Talreja.

The examiner indicates that dependent claims 7 and 15 would be allowable if rewritten in independent form.

We refer to the Final Rejection (mailed Dec. 9, 2003) and the Examiner's Answer (mailed Jun. 1, 2004) for a statement of the examiner's position and to the Brief (filed Apr. 30, 2004) and the Reply Brief (filed Jul. 30, 2004) for appellants' position with respect to the claims which stand rejected.

OPINION

The examiner has applied Koizumi against claims 1-5 and 8-13 in a § 102 rejection. Consistent with appellants' suggested grouping of claims, arguments presented, and rules in effect at the time of submission of the Brief, we select claim 1 as representative. See 37 CFR § 1.192(c)(7) (2003).

We note that appellants' specification (at 5) cites the Koizumi patent, stating that Koizumi has an OTPROM and EEPROM located on the same array, and uses one high voltage power supply. The present invention, in contrast, has separate arrays that "can be addressed separately and simultaneously."

Appellants do not contest the examiner's interpretation of representative claim 1, whereby the language regarding the high voltage generator "generating two or more different erase and write voltages" may be interpreted as requiring no more than one voltage for writing and one for erasing. The examiner finds, further, that at least the combination of the Vcg (control gate voltage) generating circuit and the Vpp (bit line voltage) generating circuit (Fig. 1) of the reference is a "high voltage generator" within the meaning of claim 1. The examiner contends that, as described at column 7 of the reference, Vpp generates a voltage of 20V for an erase operation, and Vcg generates a voltage of 0V for a write operation.

Appellants argue, in the Brief, that 0V is merely a reference signal; the high voltage generator taught by Koizumi for writing and/or erasing operates with a single voltage consisting of a 20V power signal and a 0V reference signal. The examiner, in response, reiterates that 0V can be considered a generated power supply voltage. The examiner refers, for support of the position, to column 6, lines 41 through 45 of Koizumi, which indicates that Vcg can "generate power supply voltages of 20V, 2V, and 0V in accordance with the kind of operation."

Appellants respond in turn, in the Reply Brief, that a person of ordinary skill in the art would not consider 0V to be a "generated" voltage, as 0V is a reference for terminal outputs of, for example, 5V or 20V.

We do not find appellants' theories, as set out in the Reply Brief, persuasive as to why an artisan could not consider 0V to be a generated voltage in the context of the

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Koizumi apparatus. The reference at the bottom of column 7 states that the voltage generating circuit "is set" to 0V. As the examiner notes, the output of a 0V signal must be regulated by the voltage generator. More important, however, appellants do not explain why -- while the reference expressly indicates that a power supply voltage of 0V can be generated -- the artisan somehow could not consider a power supply voltage of 0V to be "generated." We consider the objective teachings of the reference to be a better indication of the scope of the terms used in the claims, as understood by the artisan, than post hoc arguments that are contrary to the evidence in the record.

We have also considered appellants' additional comment in the Reply Brief, submitting that 0V could not be considered a "high voltage." The argument is unavailing, as claim 1 does not require that both (i.e., the minimum of two) of the generated voltages be relatively high.

We therefore sustain the rejection of claims 1-5 and 8-13 under 35 U.S.C. § 102 as being anticipated by Koizumi.

Appellants' arguments in response to the rejection of claims 6 and 14 under 35 U.S.C. § 103 as being unpatentable over Koizumi and Talreja are minimal. However, we cannot sustain the rejection because we find that a prima facie case for obviousness has not been established. The claims (e.g., claim 6) require that the operating system alternately provides the two or more different erase and write voltages to the OTPROM and the PROM array.

The rejection seems to rely on Koizumi and only on column 1, lines 43 through 63 of Talreja, with respect to a suggestion to incorporate wear-leveling in flash memory. The rejection concludes that it would have been obvious to modify the erase/write voltages to a selected PROM, as taught by Koizumi, to distribute access among flash memory blocks using wear-leveling techniques, in order to prevent degradation or failure of particular flash memory cells.

Column 1 of Talreja appears to relate that wear-leveling algorithms distribute data amongst memory blocks in a flash memory array for extending the number of programming and erasure cycles for the device; i.e., by apparent avoidance of repeated reuse of the same memory cells, to the exclusion of others, within an array. We have no showing in this record of how such algorithms might be applicable to an OTPROM (having a capability to electrically write information in the prescribed storage area only one time and no capability to erase; Koizumi col. 1, ll. 6-12). As such, we do not find suggestion for the combination that is proposed by the rejection.¹

CONCLUSION

¹ In Koizumi, the EEPROM and OTPROM regions share the same cell structure (col. 4, ll. 3-7). Consistent with instant claim 1, Koizumi teaches (col. 3, ll. 53-63) that the processor is “capable of” reading, erasing, and writing to the OTPROM region, although erasing is not performed. We note that appellants’ OTPROM as disclosed is not precisely “one time” programmable. See, e.g., spec. at 7, ll. 11-20.

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The rejection of claims 1-5 and 8-13 under 35 U.S.C. § 102 is affirmed. The rejection of claims 6 and 14 under 35 U.S.C. § 103 is reversed. The examiner's decision to reject claims 1-6 and 8-14 is thus affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a). See 37 CFR § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

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Administrative Patent Judge)	
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