

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte CHEE KIANG YEW and MASAZUMI AMAGAI

Appeal No. 2005-2530
Application No. 10/612,129¹

ON BRIEF

Before JERRY SMITH, KRASS and SAADAT, Administrative Patent Judges.
SAADAT, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the Examiner's final rejection of claims 1, 2 and 4-15. Claim 3 has been allowed and claims 16-32 have been cancelled.

We affirm.

BACKGROUND

Appellants' invention relates to a method of assembling an integrated circuit chip to an electrically insulating substrate

¹ Application for patent filed July 2, 2003, which according to Appellants, is a divisional of Application No. 09/401,572, filed September 22, 1999, now U.S. Patent No. 6,602,803.

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using a preactivated polymer adhesive layer in a variety of different semiconductor chip scale (SCS) packages.

Representative independent claim 1 is reproduced as follows:

1. A semiconductor device comprising:

an integrated circuit chip having an active and a passive surface, said active surface

including a protective polymer layer having been preactivated to impart adhesiveness, and at least one bonding pad;

an electrically insulating substrate having first and second surfaces;

a plurality of electrically conductive routing strips integral with said substrate;

a plurality of contact pads disposed on said first surface of said substrate, at least one of said contact pads electrically connected with at least one of said routing strips;

said second surface of said substrate being directly attached to said preactivated polymer layer; and

bonding wires electrically connecting said at least one bonding pad to at least one of said contact pads.

The prior art references of record relied upon by the Examiner in rejecting the appealed claims are:

<u>U.S. Patents</u>		
Lupinski et al. (Lupinski)	5,300,812	Apr. 5, 1994
Lee et al. (Lee)	6,013,946	Jan. 11, 2000 (filed Mar. 31, 1997)
<u>Japanese Published Application</u>		
Hiroshi	06-029454	Feb. 4, 1994

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Claims 1, 2, 4 and 7-15 stand rejected under 35 U.S.C. § 103 as being unpatentable over Lee and Lupinski.

Claims 5 and 6 stand rejected under 35 U.S.C. § 103 as being unpatentable over Lee, Lupinski and Hiroshi.

Rather than reiterate the opposing arguments, reference is made to the briefs and answer for the respective positions of Appellants and the Examiner. Only those arguments actually made by Appellants have been considered in this decision. Arguments which Appellants could have made but chose not to make in the briefs have not been considered (37 CFR § 41.37(c)(1)(vii)).

OPINION

With respect to the rejection of claims 1, 2, 4 and 7-15 over Lee and Lupinski, the Examiner relies on Lee for teaching a semiconductor integrated circuit chip attached to an electrically insulating substrate through a protective adhesive layer and on Lupinski for teaching a protective polymer layer for adhesion (answer, pages 3 & 4). The Examiner asserts that it would have been obvious to provide such preactivated polymer between the chip and the insulating layer to benefit from the void free adhesive bonding provided by the polymer (answer, page 4).

Appellants argue that Lupinski does not disclose a preactivated polymer layer used with an insulating substrate in

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relation with contact pads (brief, page 5). Appellants further assert that neither of the references discloses a plurality of contact pads disposed on the first surface of the substrate and the second surface of the substrate being directly attached to the polymer layer (brief, page 5; reply brief, page 2).

In response, the Examiner argues that Lupinski was relied on for teaching a preactivated polymer layer for attaching the active surface of a semiconductor chip to an insulating substrate and providing void free adhesive bonding (answer, page 7). Furthermore, the Examiner asserts that Lupinski was only relied on for using a polymer layer for adhesive bonding, and not for teaching a plurality of contact pads on the substrate being attached which is actually shown by Lee (answer, page 8) to include a protective adhesive layer used with an insulating substrate (answer, page 9).

As a general proposition, in rejecting claims under 35 U.S.C. § 103, the examiner bears the initial burden of presenting a prima facie case of obviousness. See In re Rijckaert, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993) and In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). A prima facie case of obviousness is established when the teachings of the prior art itself would appear to have suggested the

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claimed subject matter to one of ordinary skill in the art. See In re Bell, 991 F.2d 781, 783, 26 USPQ2d 1529, 1531 (Fed. Cir. 1993); In re Fritch, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992); Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir. 1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985). In considering the question of the obviousness of the claimed invention in view of the prior art relied upon, the Examiner is expected to make the factual determination set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), and to provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. See also In re Rouffet, 149 F.3d 1350, 1355, 47 USPQ2d 1453, 1456 (Fed. Cir. 1998).

A review of Lee confirms that the reference relates to a chip scale package including an insulating substrate with a first surface for bonding with the surface of a semiconductor circuit chip (col. 2, lines 17-21). As shown in Figure 2 of Lee, the top surface of a circuit substrate 120a, which includes conductive traces for connection to a semiconductor chip, is attached to the surface of semiconductor chip 130 bearing contact pads 131 using

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non-conductive adhesive layer 142 (col. 4, lines 55-59).

Lupinski, on the other hand relates to using a plasticized polymer useful as a low temperature laminating adhesive for circuit manufacturing (abstract, col. 1, lines 6-8). As depicted in the Figure, Lupinski laminates an overlay dielectric layer 50 to substrate 10 having IC chip 30 attached thereon using a plasticized polyetherimide composition 40 in order to provide void free adhesive bonding at low temperature (col. 2, lines 9-18).

Based on our findings above, we disagree with Appellants' arguments and conclusion that the combination is improper since the substrate disclosed by Lupinski has no relationship to contact pads. Both references are concerned with using an adhesive for attaching an insulating substrate to the active surface of a semiconductor chip. Specifically, as argued by the Examiner (answer, page 8), the polymeric adhesive disclosed by Lupinski provides void free adhesive bonding in a low temperature process.

We also remain unconvinced by Appellants' argument that Lupinski needs to show that insulating layer 50 includes conductive strips and contact pads on the surface to be bonded with the active surface of an integrated circuit chip for a

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proper combination with Lee. In fact, obtaining a void free adhesive bonding would have led one of ordinary skill in the art to look into the teachings of Lupinski in order to benefit from the disclosed polymeric adhesive composition for laminating an insulating substrate to an integrated circuit chip in low temperature. As in the case before us, a motivation to combine prior art references may be found in the nature of the problem to be solved. Ruiz v. A.B. Chance Co., 357 F.3d 1270, 1276, 69 USPQ2d 1686,1690 (Fed. Cir. 2004). Also, evidence of a suggestion, teaching, or motivation to modify a reference may flow from the prior art references themselves, the knowledge of one of ordinary skill in the art, or, in some cases, from the nature of the problem to be solved. See In re Dembiczak, 175 F.3d 994, 999, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999); Pro-Mold & Tool Co. v. Great Lakes Plastics, Inc., 75 F.3d 1568, 1573, 37 USPQ2d 1626, 1630 (Fed. Cir. 1996).

In view of the analysis above, we find the Examiner's reliance on the combination of Lee and Lupinski to be reasonable and sufficient to support a prima facie case of obviousness. Accordingly, the 35 U.S.C. § 103 rejection of claims 1, 2, 4 and 7-15 is sustained.

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Turning now to the 35 U.S.C. § 103 rejection of claims 5 and 6, we note Appellants' reliance on the same arguments made above with respect to claim 1. Based on our discussion above, we also find the combination of Hiroshi with Lee and Lupinski to be reasonable to support a prima facie case of obviousness. Therefore, we also sustain the 35 U.S.C. § 103 rejection of claims 5 and 6 over Lee, Lupinski and Hiroshi.

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CONCLUSION

In view of the foregoing, the decision of the Examiner rejecting claims 1, 2 and 4-15 under 35 U.S.C. § 103 is affirmed. No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a)(1)(iv).

AFFIRMED

JERRY SMITH)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
ERROL A. KRASS)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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MAHSHID D. SAADAT)	
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