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Paper 82
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

DAVID **PRUTCHI** and PATRICK J. PAUL

Junior Party
(Patent 6,525,986).

v.

KARL M.J. **LOFGREN**, JEFFREY D. STAI,
ANIL GUPTA, ROBERT D. NORMAN
and SANJAY MEHROTRA

Senior Party
(Application 10/785,373)

Patent Interference No. 105,581 (JL)
(Technology Center 2800)

Before: JAMESON LEE, RICHARD TORCZON and SALLY C. MEDLEY, *Administrative Patent Judges.*

LEE, *Administrative Patent Judge.*

Decision -- Motions -- Bd. R. 125(a)

This is a decision on Prutchi's Motions 1 and 2 and Lofgren's Motion 1. Prutchi's Motion 1, alleging unpatentability of all of Lofgren's claims corresponding to the count, i.e., claims 40-54, under 35 U.S.C. § 112, first

paragraph, for lack of written description, is **granted**. Lofgren's Motion 1, asserting unpatentability of claims 1-15 over prior art, is **dismissed**. Prutchi's Motion 2 attacking the priority benefit initially accorded Lofgren is also **dismissed**.

Findings of Fact

These enumerated findings, as well as all other findings contained in the discussion portion of this opinion, are supported by a preponderance of the evidence.

1. This interference was declared on October 1, 2007. (Paper 1)
2. Lofgren is involved on the basis of Application 10/785,373, filed February 23, 2004. (Paper 1)
3. Prutchi is involved on the basis of Patent 6,525,986, based on Application 09/767,040, filed January 22, 2001.
4. Lofgren's real party in interest is SanDisk Corporation and Western Digital Corporation. (Paper 10)
5. Prutchi's real party in interest is Intermedics, Inc. (Paper 5)
6. The count of the interference is defined as Lofgren's Application claim 40 or claim 51, or Prutchi's Patent claim 1 or claim 12. (Paper 1)
7. Lofgren has been accorded benefit of the following applications:

   Application 09/939,290, filed August 22, 2001;
   Application 09/657,369, filed September 8, 2000;
   Application 09/064,528, filed April 21, 1998;
   Application 08/931,193, filed September 16, 1997;
   Application 07/736,733, filed July 26, 1991; and

Application 08/396,488, filed March 2, 1995.

8. Prutchi has been accorded benefit of the following applications:

Application 09/347,841, filed July 2, 1999; and

Application 08/903,313, filed July 30, 1997.

9. All of Lofgren's involved application claims 40-54 were added by preliminary amendment which represented that the added claims 45-54 are "exact copies of claims 1-15" of Prutchi's involved Patent 6,525,986.

10. Of Lofgren's involved claims 40-54, only claims 40, 45, and 51 are independent claims, as reproduced below:

Claim 40. A method comprising:

> receiving an address at each of a plurality of memory chips, the plurality of memory chips including a first memory chip having a first programmable code and a second memory chip having a second programmable code, wherein the first programmable code is different from the second programmable code;
>
> enabling the first memory chip based on a comparison of a portion of the received address with the first programmable code; and
>
> disabling the second memory chip based on a comparison of the portion of the received address with the second programmable code.

Claim 45. A method comprising:

> assigning a first selection code to a first memory chip and a second selection code to a second memory chip, wherein the second selection code differs from the first selection code;

receiving a portion of an address at the first memory chip and at the second memory chip;

comparing the portion of the address to the first selection code and to the second selection code; and

enabling the first memory chip and disabling the second memory chip based on the comparison.

Claim 51. A method comprising:

coupling a plurality of address lines of a first memory chip in parallel with a plurality of address lines of a second memory chip;

setting a first code at the first memory chip;

receiving a portion of an address at the first memory chip;

enabling the first memory chip if the received address portion matches the first code; and

otherwise disabling the first memory chip.

10. Lofgren's disclosed invention is directed to a device and method for controlling solid-state memory. (Exhibit 2004).

11. Lofgren's specification describes that "[a]n important aspect of the invention is to employ a broadcast select scheme to select or enable a given memory device chip among an array of chips in a memory board or memory module." (Exhibit 2004, ¶ 16, ll. 1-3).

12. Lofgren's specification describes that to select a given memory chip, the correct array address for that chip is sent to all the memory chips to be

compared at each chip with the chip's own address, and that "the chip that matched is selected or enabled by its device select circuit." (Exhibit 2004, ¶ 16, ll. 11-12).

13. Lofgren's specification describes that "each memory chip can be addressed for selection or enablement." (Exhibit 2004, ¶50, ll. 3-4).

14. Each of the above-noted description in Lofgren's specification uses the terms "select" and "enable" or "selection" and "enablement" in an equivalent manner without distinction in the context of an action performed on a memory chip.

15. Lofgren's specification describes that "[a] memory chip remains selected until explicitly deselected, allowing more than one memory chip to be enabled at a time." (Exhibit 2004, ¶ 16, ll. 13-14).

16. The statement quoted in FF. 15 indicates that a selected memory is an enabled memory and again supports a reading which makes no distinction between "select" and "enable."

17. Lofgren's specification states (Exhibit 2004, ¶ 17, ll. 3-5): "This also avoids the need for conventional use of using conventional individual chip select to enable each memory chip."

18. The statement quoted in FF. 17 indicates that "select" is to "enable," and again supports a reading which makes no distinction between "select" and "enable."

19. Lofgren's specification states (Exhibit 2004, ¶ 44, ll. 4-6): "The one or more memory modules such as 131, 132 can be selectively enabled by individual module select signals such as MS1*, MS2*."

20. The statement quoted in FF.19 indicates that a select signal enables and again supports a reading which makes no distinction between "select" and "enable."

21. Lofgren's specification states (Exhibit 2004, ¶ 54, ll. 1-3): "[O]ne particular 'key' among the permutations of grounding configurations of the multi-bit mounts 149 is reserved as a 'master select' which unconditionally allows each chip to be selected or enabled."

22. The statement quoted in FF. 21 indicates that "select" is "select" or "enable," and again supports a reading which makes no distinction between "select" and "enable."

23. Lofgren's specification states (Exhibit 2004, ¶ 18, ll. 2-3): "Each of the memory modules can be enabled by a module select signal from the controller module."

24. The statement quoted in FF. 23 indicates that a select signal enables a memory module, and again supports a reading which makes no distinction between "select" and "enable."

25. The only description in Lofgren's specification, which arguably can be read, in isolation, as making a substantive distinction between "enable" and "select" is this (Exhibit 2004, ¶ 62, ll. 1-3): "[A]ny memory device 141 among the array of memory devices mounted on the backplane 143 may be enabled such that the device is selected whenever the CS*171 (chip select) is asserted."

26. The CS*171 chip select signal is a clock signal the trailing edge of which triggers the address-match latch 307 shown in Lofgren's Figure 5A to latch

a data input that is provided from the output of comparator 305. (Exhibit 2004, ¶ 69, ll. 9-10).

27. Lofgren's Figure 5A, which illustrates one of many identical device select circuits operating in parallel and one for each associated memory chip, is reproduced below:

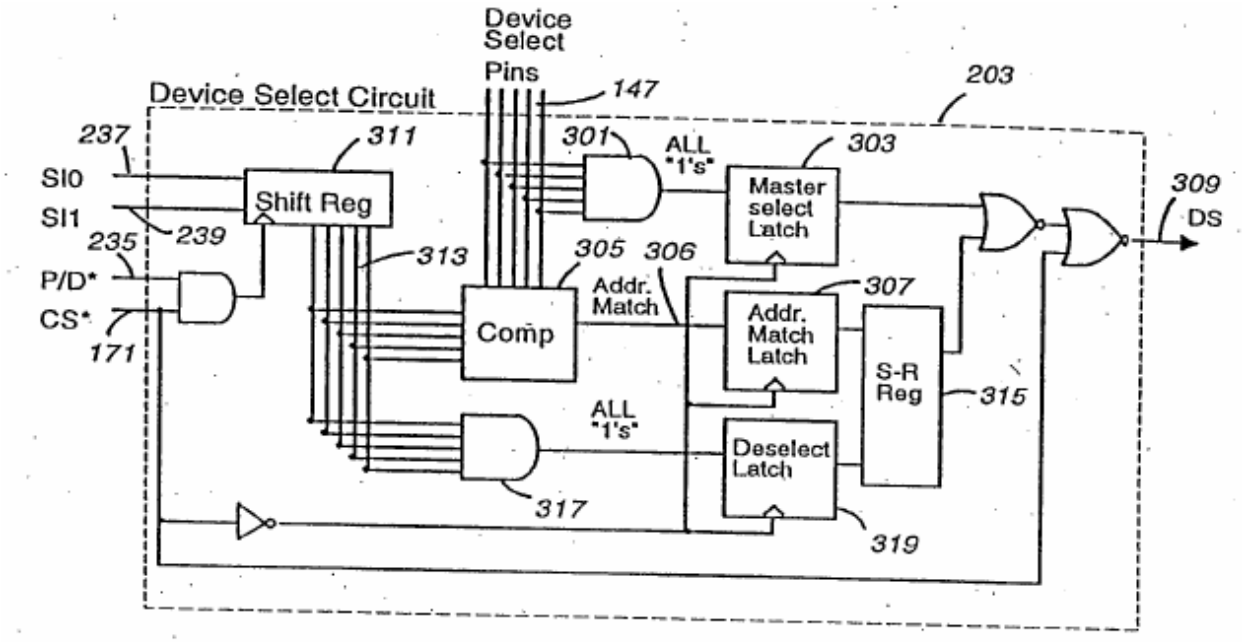

Fig. 5A

Lofgren's Figure 5A depicts one of many identical device select circuits operating in parallel and one for each associated memory chip.

28. The address-match latch 307 does not latch its data input continually, but only upon the occurrence of the trailing edge of signal CS*171. (Exhibit 2004, ¶ 69, ll. 9-10).

29. When the CS*171 signal initially goes high, a 5-bit array address is shifted into shift register 311. (Exhibit 2004, ¶ 69, ll. 4-6).

30. Before the CS*171 signal goes low, the 5-bit array address is passed from the shift register to the comparator 305 and the comparator compares the 5-bit address with its own address obtained from pinouts 147 to provide a high output if there is a match. (Exhibit 2004, ¶ 69, ll. 6-9).

31. A high output from comparator 305 on line 306 signals an address match and would be clocked into the address-match latch 307 by the falling edge of signal CS*171. (Exhibit 2004, ¶ 69, ll. 9-10).

32. The high output latched by address match latch 307 results in the S-R register 315 being set high to yield a high at DS 309, thus "selecting" the associated memory chip whose address has been matched. (Exhibit 2004, ¶ 69, ll. 10-11).

33. If the comparator does not yield a positive address match, its output will not cause address match latch 307 to latch a high and thus DS 309 will not be caused to go from low to high to select an associated memory chip whose address has not been matched. (Exhibit 2004, ¶ 69, ll. 11-12).

34. The statement quoted in FF.25 is also consistent with there being no distinction between "select" and "enable," whereby the reference to the CS*171 chip select signal merely indicates the precise timing of when the associated

memory chip is selected or enabled, and that meaning comports with how the two terms are used elsewhere in the specification.

35. The terms “select” and “enable” are consistently used equivalently and interchangeably throughout Lofgren’s specification. (FF. 11-24, 34).

36. The S-R register 315 is a set-reset register set by a high signal on the input that is connected to the address match latch 307 and reset by a high signal on the input that is connected to the deselect latch 319. (Oral Arg. Transcript 31:18 to 32:6).

37. A low signal on that input of the S-R register 315 which is connected to the address match latch does not reset the S-R register. (Oral Arg. Transcript 31:18 to 32:6).

38. The Lofgren specification (Exhibit 2004) does not use the word ”disable” or “disabling” to refer to any action performed on a memory device, except in claim 21, an original claim, which reads:

> A mass storage system as in claim 11, wherein said device select circuit further including:
>
> a device deselect circuit for disabling each memory chip thereof whenever an array address received from the device bus coincides with a predetermined address.

39. The written description part of Lofgren specification (Exhibit 2004) discusses and refers only to deselecting a memory device and deselected memory devices, not disabling a memory device.

40. The Lofgren specification states (Exhibit 2004, ¶ 65, ll. 1-4): “According to yet another aspect of the invention, an ‘address deselect’ [‘address

deselect'] scheme is employed in which a special address or code can be shifted in to deselect devices that have previously been selected. In the preferred embodiment, the special deselect code is (11111)."

41. The statement quoted in FF. 40 indicates that a single deselect code operates to deselect all devices which have previously been selected.

42. With regard to deselecting memory devices, the Lofgren specification states (Exhibit 2004, ¶ 70, ll. 1-8):

> Device deselection by "address-deselect" "address deselect" which is implemented by a special deselect code e.g., (11111) is used to signal global deselection. A second 5-input AND gate 317 looks for a data pattern of all one's being shifted into the shift register 311. When a match occurs and also the chip select CS* in the line 171 is activated goes from HIGH to LOW (see Fig. 5B), the comparator 317 outputs a deselect signal which is latched by a deselect latch 319. This in turn is used to reset the S-R register 315 on all devices previously selected. By shifting in the (11111) pattern and activating the CS* signal, all devices that are presently selected will see the deselect pattern and will be deselected.

43. The text quoted in FF. 42 describes that a single special code, e.g., (11111), causes deselection of all memory devices which have been previously selected, and that it is done in each control circuit associated with a corresponding memory device through a 5-bit AND gate 317 which feeds into deselect latch 319 that is connected to the reset input terminal of the S-R register 315.

44. The high output of deselect latch 319 resets the S-R register 315 to cause the ultimate output DS 309 to be low, thus deselecting the associated memory device. (FF. 42-43).

45. A high signal on DS 309 selects the associated memory and a low signal on DS 309 deselects the associated memory. (FF. 28-32 and 40-44).

46. The special code for global deselection deselects all memory devices which have previously been selected and has nothing to do with setting the S-R register to cause the selection of any memory device. (Exhibit 2004, ¶ 70, ll. 1-8).

47. The output of comparator 305 does not influence the content of deselect latch 319 and therefore has no effect on S-R register's reset terminal used to cause the deselection of the associated memory device. (Exhibit 2004, Fig. 5A).

Discussion

A. Prutchi's Motion 1

Prutchi asserts that Lofgren's claims 40-54 are unpatentable under 35 U.S.C. § 112, first paragraph, for lack of written description in the specification. The test for written description under 35 U.S.C. § 112, is whether the specification reasonably would have conveyed to one with ordinary skill in the art that "the inventor possessed the invention at the time of that original disclosure." *E.g.*, *Pandrol USA, LP v. Airboss Ry. Products, Inc.*, 424 F.3d 1161, 1165 (Fed. Cir. 2005); *Vas-Cath Inc. v. Mahurkar*, 935 F.2d 1555, 1563-64 (Fed. Cir. 1991).

Independent claims 40 and 45 require the steps of enabling a memory chip and disabling a memory chip on the basis of a comparison involving the same received address portion.

For instance, claim 40 requires (1) enabling a first memory chip based on the comparison of the received address portion with a first code and (2) disabling a second memory chip based on the comparison of the received address portion with a second code. Claim 45 requires (1) enabling a first memory chip and (2)

disabling a second memory chip, based on the comparison of the received address portion with a first and a second code.

Claim 51 requires enabling a memory chip if the received address portion matches a first code and disabling the memory chip if there is not a match.

Prutchi's summary of the claims as all requiring the ability to enable <u>and</u> disable a memory chip based on a single address (Motion 1 6:20-21) is correct and not disputed by Lofgren.

Lofgren's specification uses the terms "select" and "enable" in an equivalent and interchangeable manner throughout the specification, within the context of an action performed on a memory device. (FF. 14, 16, 18, 20, 22, 24, 34, 35). We interpret "enable" in the context of Lofgren's claims as having the same meaning as "select" insofar as it is directed to an action done on a memory device.

While it is argued by Lofgren that the following sentence in its specification (Exhibit 2004, ¶ 62, ll. 1-3) means that enable refers to the placing of a high output from comparator 305 on the input of address match latch 307 and select does not occur until a little later upon occurrence of the trailing edge of the chip select signal CS*171, we do not so find: "[A]ny memory device 141 among the array of memory devices mounted on the backplane 143 may be enabled such that the device is selected whenever the CS*171 (chip select) is asserted." The distinction made by Lofgren between "enable" and "select" is strained and not meaningful, as Lofgren has not pointed to any action which takes place in the short duration between the outputting of a high signal from comparator 305 and the occurrence of the trailing edge of signal CS*171. In light of all the other portions of Lofgren's specification which make no distinction between "enable" and "select," we read

the above-quoted sentence also as conveying that "enable" and "select" mean the same. The reference to assertion of chip select signal CS*171 only additionally explains when enablement or selection is precisely deemed to have occurred, i.e., upon assertion of the CS*171 signal. That reading is reasonable and entirely consistent with the rest of Lofgren's specification.

Testifying on cross-examination, Lofgren's technical witness Richard Simko recognizes and does not deny that in various portions of the specification the terms "enable" and "select" are used interchangeably. (Exhibit 2026; pages 127-134). Rather, he submits that such apparent expressions of interchangeability are inaccurate in light of the distinction made in ¶ 62 of the specification, which we have already identified and discussed above. In short, he dismisses a plethora of indications of interchangeability as inaccurate or wrong, based on a single instance where the two terms are arguably not interchangeable. We do not credit his testimony in that regard, because he does not explain why it is not his interpretation of ¶ 62 of the specification which would be wrong in light of the rest of the specification. Paragraph 62 of Lofgren's specification does not have to be read as creating a conflict with the rest of the specification. There is an alternative and reasonable reading which is consistent with interchangeability of the terms "enable" and "select" as we have already discussed above.

Prutchi's motion recognizes that the Lofgren specification contains a written description of enabling a memory chip based on a comparison of the received address portion with a given code. Specifically, according to Lofgren's specification, memory device selection by address-matching is implemented by the comparator 305 and the address-match latch 307. (Exh. 2004, ¶ 69, ll. 1-2). A 5-

bit array address as a received address portion is shifted into shift register 311 (FF. 29) and then passed to the comparator 305 which compares that received address portion with its own address obtained from pinouts 147 and provides a high on output line 306 when there is a match (FF. 30). The high output on line 306 is clocked into the address-match latch 307 by the falling edge of CS* 171. (FF. 31). That results in the set-reset register (S-R register) 315 being set to high to yield a high at DS 309, thus selecting the associated memory chip whose address has been matched. (FF. 32).

It is Prutchi's position that given that Lofgren's specification uses the terms "enable" and "select" in an equivalent and interchangeable manner in the context of a memory chip, any description in Lofgren's specification about disabling a memory would have to be the description on deselecting a memory chip. We find only one instance in Lofgren's application, as filed, where the term "disable" or "disabling" is used in connection with an action performed on a memory device, and that is in original claim 21 which reads:

> 21. A mass storage system as in claim 11, wherein said device select circuit further including:
>
> a device **deselect circuit for disabling** each memory chip thereof whenever an array address received from the device bus coincides with a predetermined address. (Emphasis added).

Prutchi's reasoning is logical and its position is in full agreement with the only text in Lofgren's application as filed which refers to "disabling" a memory. Note that as is recited in claim 21 quoted above, it is the "deselect circuit" which is for

disabling a memory chip. Lofgren has not pointed to any other instance in its original disclosure where the term “disable” or “disabling” is used to describe action taken on a memory chip.

Prutchi’s motion discusses how Lofgren’s disclosure of how a memory chip is deselected reveals that the Lofgren specification does not have written description for the ability to enable and disable a memory chip on the basis of a single received address as is required by the Lofgren claims. The argument is persuasive. Memory chip selection and memory chip deselection, which represent memory chip enabling and disabling in the context of Lofgren’s specification, are not based on the same received memory address.

The S-R register 315 shown in Lofgren’s Figure 5A reproduced above is a set-reset register set by a high signal on the input connected to the address match latch 307 and reset by a high signal on the input connected to the deselect latch 319. (FF. 36). To deselect a memory device, a special 5-bit global deselect code such as “11111” is shifted into shift register 311 whose special deselect data pattern is detected by the 5-input AND gate 317 which then outputs a deselect signal latched by deselect latch 319. (FF. 42-43). The high output of deselect latch 319 resets the S-R register 315 to cause the ultimate output DS 309 to be low, thus deselecting the associated memory device. (FF. 44). Because the deselect code is global, all memory chips are deselected at the same time upon receipt of the deselect code. Note that Figure 5A illustrates the control circuit for each memory chip and thus there is a separate circuit like that shown in Figure 5A for each memory chip.

The pathway to memory chip selection is from shift register 311, to comparator 305, to the address match latch 307, to the set input of the S-R register 315, and ultimately to a high output at DS 309. The pathway to memory chip deselection is from shift register 311, to AND gate 317, to deselect latch 319, to the reset input of S-R register 315, and ultimately to a low output at DS 309. The two are independent of each other.

In Lofgren's specification, the global deselect code is for deselecting all memory chips and thus is ineffective to cause the selection of any memory chip. Also, all memory chip deselection occurs through application of the global deselect code. Consequently, any address capable of selecting a memory chip is ineffective to cause the deselection of any memory chip. There is no mixing of memory chip selection with memory chip deselection, per received address. The same received address portion cannot result in both the selection of one memory chip and the deselection of another. Therefore, the claim feature in claims 40 and 45 of enabling a memory chip and disabling a memory chip on the basis of a comparison involving the same received address portion is not described. As for claim 51, it requires enabling a memory chip when the received address matches a first code and otherwise disabling the memory chip, i.e., when there is <u>not a match</u>. Because Lofgren's specification discloses memory chip deselection only when the received address portion <u>matches</u> a global deselect code, a code which is incapable of causing enablement of any memory whether it is matched or not, the subject matter of claim 51 is also not described. As is the case with claims 45 and 50, claim 51 requires the ability to enable and disable a memory chip on the basis of a single received address portion.

In the alternative, our conclusion of lack of written description for the claimed invention is unchanged even if, as argued by Lofgren, enabling a memory means something different from selecting a memory. According to Lofgren, simply providing a high output from comparator 305 on line 306 to the input of address match latch 307 constitutes enabling the corresponding memory chip even though the trailing edge of chip select signal CS*171 has not yet occurred. Also, according to Lofgren, providing a low output from comparator 305 on line 306 to the input of address match 307 constitutes disabling the corresponding memory chip. Under that view, both enabling and disabling of a memory chip is based on the results of a comparison operation at the comparator 305 in connection with a single address. However, both of Lofgren's assertions, one regarding enabling the memory and the other regarding disabling a memory, are without merit and thus rejected.

Enabling a memory chip must have some substantive meaning. Disabling a memory chip also must have some substantive meaning. We agree with the meaning first put forth by Lofgren's technical witness Richard Simko, which meaning is not disputed by Prutchi.

Paragraph 16 of Richard Simko's declaration (Exhibit 1016) states:

> 16. According to Webster's Third New International Dictionary (Merriam-Webster, Inc. 2002) ("Webster's), "to enable" is understood to mean, among other things, "to make possible, practical or easy," Exh. 1008 at 3. Based on my knowledge and experience, engineers view the ordinary and customary meaning of "to enable" to also include "to cause to function."

Paragraph 23 of Richard Simko's declaration (Exhibit 1016) states:

> 23. According to Webster's, "to disable" is understood to mean, among other things, "to make" incapable or ineffective." Exh. 1009 at 3. Based on my knowledge and experience as an engineer, the ordinary and customary meaning of "to disable" also includes "to cause not to function."

The meaning of "enable" as "to cause to function" is consistent with Lofgren's specification, which in Paragraph 72 states: "After a memory device 141 (see Figs. 2, 3, 4) has been addressed and enabled, read or write operations may be performed on it."

On cross examination (Exhibit 2026, 149:5 to 150:21), Mr. Simko changed his testimony regarding the meaning of "to enable" and "to disable," and said that the changed definition would "better fit" what is going on in a two-step address-select scheme such as that disclosed in Lofgren. Mr. Simko did not explain what he means by a "better fit," which is a nebulous term, why the revised meaning would be a "better fit," or even whether the "better fit" would be from the perspective of one with ordinary skill in the art. Moreover, whatever "better fit" means, it does not indicate that the meaning according to Mr. Simko's original testimony would "not" fit. We do not take lightly the revision by a party's own technical witness of his own previously held position regarding the ordinary and customary meaning of key claim terms, possibly to avoid the adverse consequences resulting from the original position. Where the issue is whether Lofgren's specification provides adequate written description for the claimed invention under 35 U.S.C. § 112, first paragraph, the conclusory and nebulous justification offered by Mr. Simko, i.e., that his revised position is a "better fit" to Lofgren's disclosed

invention, is particularly suspect. In the absence of an adequate explanation of the change in his position, which is the case here, we do not credit the revised testimony of Mr. Simko concerning the meaning of "to enable" and "disable," and will credit, instead, Mr. Simko's original testimony on the meaning of those terms.

By "to cause to function" it is implicit that the device caused to function was not already in the desirable functioning state. Similarly, by "to cause not to function," it is also implicit that the device caused not to function was not already in the desirable non-functioning state. We reject Lofgren's position that when a memory chip is already enabled, an action which maintains the status quo and which does not cause any change can be deemed as enabling the memory chip. We also reject Lofgren's position that when a memory chip is already disabled, an action which maintains the status quo and which does not cause any change can be deemed as disabling the memory chip.

To satisfy the written description requirement under 35 U.S.C. § 112, first paragraph, Lofgren's specification must describe enabling a memory chip which is not already enabled, and disabling a memory chip which is not already disabled, based on the same received address portion. The specification must describe a non-functioning memory chip which is caused to function, and a functioning memory chip which is caused not to function, based on a single address portion.

Simply placing a high output from comparator 305 on line 306 for input to address match latch 307 does not cause that input to be latched because address match latch 307 latches data only on the trailing edge of the chip select signal CS*171. (FF. 28). At oral argument, counsel for Lofgren recognized the same. (Oral Arg. Transcript 32:10-21). Accordingly, during the time from when a high

output from comparator 305 is provided onto line 306 and the time of occurrence of the trailing edge of chip select signal CS*171, nothing happens to the corresponding memory chip on the basis of the high output from the comparator. During that time, a corresponding not-yet functioning memory chip is unaffected and not caused to do anything different from whatever it was already doing or not doing. Lofgren's argument that simply providing a high output from comparator 305 onto line 306 for input to address match latch 307 enables the corresponding memory chip, prior to occurrence of the trailing edge of chip select signal CS*171, is without merit. The enabling referred to by Lofgren, which allegedly occurs prior to selecting a memory upon the trailing edge of the chip select signal CS*171, is fictitious and does not exist.

As for the alleged disabling of a memory chip, placing a low output from comparator 305 onto line 306 for input to address match 307 does not have any effect or influence on a corresponding memory chip, either before or after the trailing edge of the chip select CS*171 signal. That is because the output of address match latch 307 is connected to the set input and not the reset input of S-R register 315. A low input provided to the set input of S-R register 315 does not cause any change in the state of the S-R register. The S-R register is set by a high at its set input and is reset by a high at its reset input. (FF. 36). A low provided to the set input simply maintains the status quo and does not either set or reset the S-R register to cause any change in the operability of a corresponding memory chip. (FF. 37, 38). Lofgren has not pointed to or identified any resulting effect on the function or operability of a corresponding memory chip stemming from the

placement of a low output from comparator 305 onto line 306. The disabling action referred to by Lofgren is also fictitious and simply does not exist.

We further reject Lofgren's assumption that if placing a high on a signal line means enabling a memory, then placing a low on the same line would mean disabling the memory. It does not necessarily follow that that would be the case. Whether it is so depends on an analysis of what happens to the corresponding memory chip when a high is placed on the line and what happens when a low is placed on the same line. As discussed above, simply placing a high on line 306 from the output of comparator 305 is not sufficient to enable a memory prior to occurrence of the trailing edge of chip select signal CS*171, and placing a low on line 306 from the output of comparator 305 is ineffective to disable any memory chip prior to or subsequent to the occurrence of the trailing edge of chip select signal CS*171. Furthermore, Lofgren's original disclosure through claim 21 already describes disabling of a memory chip as something performed by the memory deselect circuit. In light of that disclosure, there is no reason to characterize by deduction, speculation, and assumption something outside of the deselect circuit as performing memory disabling when nothing in the specification so indicates.

For the foregoing reasons, Lofgren's claims 40-54 are unpatentable for lack of written description as is required by 35 U.S.C. § 112, first paragraph.

B. Prutchi's Motion 2

Prutchi's Motion 2 attacks the priority benefit initially accorded Lofgren to Patent 6,715,044, filed August 22, 2001, Patent 6,317,812, filed September 8, 2000, Patent 6,148,363, filed April 21, 1998, Patent 5,806,070, filed September

16, 1997, Patent 5,430,859, filed July 26, 1991, and Application 08/396,488, filed March 2, 1995. We do not reach the merits of this motion because in light of the granting of Prutchi's Motion 1, there will be no priority determination in this interference. Judgment is entered against Lofgren in a concurrent paper.

C. Lofgren's Motion 1

Lofgren's Motion 1 asserts unpatentability of Prutchi's claims 1-15 over prior art. We do not reach the merits of this motion because in light of the granting of Prutchi's Motion 1, which raised a threshold issue, Lofgren is without standing to proceed further in this interference.

Conclusion

Prutchi's Motion 1 is **granted**.

Prutchi's Motion 2 is **dismissed**.

Lofgren's Motion 1 is **dismissed**.

Judgment will be entered against Lofgren in a separate paper.

By Electronic Transmission:

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