The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 100

UNITED STATES PATENT AND TRADEMARK OFFICE

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U.S. PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS
AND INTERFERENCES

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte TRANSLOGIC TECHNOLOGY, INC.

Appeal No. 2005-1050
Reexamination Control Nos. 90/005,384,
90/005,823, 90/005,881, 90/006,051,
and 90/006,392

HEARD: May 31, 2005

Before KRASS, BARRETT, and NAPPI, Administrative Patent Judges.

BARRETT, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. §§ 306 and 134(b) from the final rejection of claims 16, 17, 39-45, 47, and 48, all of the pending claims. Patent claims 1-15 and 18-27 have been canceled and claims 28-38 and 46 added during the reexaminations have been canceled.

We affirm.

REEXAMINATIONS

This appeal involves five merged reexamination proceedings for reexamination of U.S. Patent 5,162,666 ('666 patent), entitled "Transmission Gate Series Multiplexer," issued November 10, 1992, to Dzung J. Tran, based on application 07/670,075, filed March 15, 1991, now assigned to Translogic Technology, Inc., 7353 S.E. Hacienda, Hillsboro, Oregon, 97123.

Reexamination Control No. 90/005,384 was filed June 4, 1999, by a third party requester, Alan R. Loudermilk.

Reexamination Control No. 90/005,823 was filed September 26, 2000, by third party requester Alan R. Loudermilk and merged with the first reexamination proceeding.

Reexamination Control No. 90/005,881 was filed December 8, 2000, by third party requester Alan R. Loudermilk and merged with the first two reexamination proceedings.

Reexamination Control No. 90/006,051 was filed July 3, 2001, by the patent owner, Translogic Technology, Inc. (TTI), and merged with the first three reexamination proceedings.

Reexamination Control No. 90/006,392 was filed September 27, 2002, by third party requester Alan R. Loudermilk and merged with the first four reexamination proceedings.

RELATED LITIGATION

The '666 patent is the subject of Translogic Technology, Inc. v. Hitachi, Ltd., No. 99-407-PA (D. Ore. filed March 24, 1999). A jury verdict was signed on October 27, 2003, and entered on October 29, 2003, determining that Hitachi had not proved by clear and convincing evidence that claims 16 and 17 of the '666 patent were invalid for anticipation or obviousness. On February 22, 2005, the district court adopted a special master's report and recommendation on infringement finding infringement of claims 16 and 17 of the '666 patent and granted plaintiff's motion for summary judgment of infringement. A jury verdict was signed on May 6, 2005, and entered on May 10, 2005, finding inducement of infringement of claims 16 and 17, and awarding damages of $86.5 million. An order granting plaintiff's motion for a permanent injunction and denying defendant's motion for a stay was signed on May 12, 2005, and entered on May 13, 2005. A notice of appeal and an emergency motion for stay of the permanent injunction pending appeal were filed in the U.S. Court of Appeals for the Federal Circuit on May 12, 2005.

BACKGROUND

The invention relates to a type of digital logic circuit known as a "multiplexer," or "MUX" for short. A multiplexer circuit has one or more control inputs that control the device to

select one of several data inputs to connect to a single output line. A conventional k:1 multiplexer with p control lines selects one of $k=2^p$ data input lines to connect to a single output line; e.g., a 2:1 multiplexer has one control input and two data inputs, a 4:1 multiplexer has two control inputs and four data inputs, etc.

The claims on appeal are directed to a multiplexer having three or four 2:1 transmission gate multiplexers (TGMs) connected in series, that is, with the output of a TGM connected to one input of the next TGM. Each TGM in the series is called a "stage." A TGM is constructed using transmission gates (TGs), which are electronic circuits that pass the input (a logical "0" or "1") to the output when the control input is a logical "1" and block the input when the control input is a logical "0." A multiplexer constructed from a series of TGMs has p control inputs and (p+1) data inputs for total of (2p+1) inputs; thus, a series 4:1 multiplexer has p=3 control inputs instead of 2 control inputs as in a conventional multiplexer.

Representative claims 47 is reproduced below.

47. A multiplexer circuit comprising:

a first stage TGM circuit having first and second signal input terminals, a control input terminal and an output terminal;

the first and second signal input terminals coupled to receive first and second input variables, respectively;

the control input coupled to receive a first control signal;

a second stage TGM circuit having first and second signal input terminals, a control input terminal and an output terminal;

one of the second stage input terminals coupled to the first stage output terminal;

the other one of the second stage input terminals coupled to receive a third input variable;

the second stage control input terminal coupled to receive a second control signal;

a third stage TGM circuit having first and second signal input terminals, a control input terminal and an output terminal;

one of the third stage input terminals coupled to the second stage output terminal;

the other one of the third stage input terminals coupled to receive a fourth input variable; and

the third stage control input terminal coupled to receive a third control signal;

whereby the circuit forms a 4:1 multiplexer.

THE REFERENCES

The examiner relies on the following references:

Tosser, A.J., and Aoulad-Syad, D. ("Tosser"), Cascade networks of logic functions built in multiplexer units, IEE Proc., Vol. 127, Pt. E, No. 2, March 1980, pages 64-68.

Weste, Neil H.E., and Eshraghian, Kamran ("Weste"), Principles of CMOS VLSI Design: A Systems Perspective (1985 Addison-Wesley Publ. Co.), pages 14-17 and 172-175.

Gorai, R.K., and Pal, A. ("Gorai"), Automated synthesis of combinational circuits by cascade networks of multiplexers, IEEE Proc., Vol. 137, Pt. E, No. 2, March 1990, pages 164-170.

THE REJECTIONS

Pages of the final rejection are referred to as "FR__" and pages of the examiner's answer are referred to as "EA__." Pages of the appeal brief are referred to as "Br__" and pages of the reply brief are referred to as "RBr__."

Claims 16, 17, 39-45, 47, and 48 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Gorai and Weste. The examiner finds that Fig. 3 of Gorai teaches a three-stage multiplexer with four input signals (h_p, g_p, h_{p-1}, h_1) and three control signals (x_p, x_{p-1}, and x_1) (FR2). The examiner finds that Gorai does not disclose that the multiplexers are transmission gate multiplexers (TGMs) (FR2-3). The examiner finds that Weste teaches 2:1 TGM circuits which transfer full logic "0" or "1" signals between the input and output (FR3). The examiner

concludes that one of ordinary skill in the art would have been motivated to use the TGM circuit in Weste for the multiplexers in Gorai for this reason (FR3). The examiner also finds that the fact that Gorai only shows "black boxes" for the multiplexer stages would have suggested to one skilled in the art to use any conventional multiplexer circuit, such as the TGM taught by Weste (FR3-4). The examiner finds that Fig. 3 of Gorai is a network of *p* stages, which suggests any number of cascaded multiplexers, including the 4-stage multiplexer of claim 48 (FR4).

Claims 16, 17, 39-45, 47, and 48 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tosser and Weste. The examiner finds that Fig. 9 of Tosser teaches a 4:1 multiplexer having three cascaded 2:1 multiplexer stages (FR5). The examiner finds that Tosser does not disclose that multiplexers are implemented using TGMs (FR5). The examiner finds that Weste teaches 2:1 TGM circuits which transfer full logic "0" or "1" signals between the input and output (FR5). The examiner concludes that one of ordinary skill in the art would have been motivated to use the TGM circuit in Weste for the multiplexers in Tosser for this reason (FR5-6). The examiner also finds that the fact that Tosser only shows "black boxes" for the multiplexer stages would have suggested to one of ordinary skill in the art to use any conventional multiplexer circuit,

such as the TGM taught by Weste (FR6). The examiner concludes that it would have been obvious to add an additional stage to the multiplexers to allow processing of more input signals (FR7).

OPINION

Grouping of claims

Patent owner states that claim 47 is representative of the 4:1 multiplexer claims 16, 39-41, 45, and 47, and that claim 48 is representative of the 5:1 multiplexer claims 17, 42-44, and 48 (Br11). This grouping of claims was confirmed at the oral hearing. Claims 47 and 48 correspond to original patent claims 16 and 17 in the '666 patent, rewritten in independent form, which were held not invalid and infringed in Translogic v. Hitachi. Thus, claims 16, 39-41, 45, and 47 stand or fall together with claim 47, and claims 17, 42-44, and 48 stand or fall together with claim 48.

Claim interpretation

The following is an interpretation of terms in claims 47 and 48. The interpretation is consistent with that in the claim construction attached to the Order of May 12, 2005, in Translogic v. Hitachi, except for the interpretations of "one of the fourth stage input terminals coupled to the third stage output

terminal," and like limitations, which are unimportant to the analysis and the outcome. Several additional terms are defined.

TERM	INTERPRETATION
"multiplexer"	A circuit that accepts a plural number (N) of input signals and, based on the state of control signals that are received by the multiplexer, selects as an output a single one of the input signals.
"comprising"	"'Comprising' is a term of art used in claim language which means that the named elements are essential, but other elements may be added and still form a construct within the scope of the claim." Genentech, Inc. v. Chiron Corp., 112 F.3d 495, 501, 42 USPQ2d 1608, 1633 (Fed. Cir. 1997).
"TGM" or "TGM circuit"	A 2:1 multiplexer comprising a pair of transmission gates together with their associated control input and inverter, with the outputs of the transmission gates connected together ('666 patent, col. 2, lines 63-66). Each of the transmission gates may consist of a single pass transistor or a complementary pair of transistors ('666 patent, col. 1, lines 46-50).
"control signal"	A signal applied to a TGM control input terminal that controls the TGM to select one of the two input terminals for connection to the output terminal. This construction does not preclude the control signal from being used to control another TGM outside of the claimed multiplexer. Compare claim 42 (not argued) which recites "wherein TGM circuit loading on the first control signal consists of a single TGM circuit," which precludes applying the control signal to another TGM.

first, second, third, and fourth "control signals"	In a multiplexer circuit, these control signals are unique and independent of each other. However, the actual control signals are not part of the claimed multiplexer structure.
signal input terminal "coupled to" a previous stage output terminal	Connected to, directly or through one or more intervening inverters or buffers.
control input terminal "coupled to receive" a control signal	Terminal capable of receiving a control signal. The control signal itself is not part of the claimed structure.
"input variable"	A signal to be input to one of the input terminals of a TGM. Patent owner agrees that the "input variable" itself is not part of the claimed structure (RBr14). A "variable" is defined as: "A symbol used to represent an unspecified member of some set. A variable is a 'place holder' or a 'blank' for the name of some member of the set. Any member of the set is a **value** of the variable and the set itself is the **range** of the variable. If the set has only one member, the variable is a **constant**." James and James, Mathematics Dictionary (5th ed. Chapman & Hall 1992). A "variable" is also defined as: "**1:** something that is variable **2 a:** a quantity that may assume any one of a set of values **b:** symbol representing a variable." Webster's New Collegiate Dictionary (G.&C. Merriam Co. 1977). Thus, a "variable" does not necessarily imply a variation in value over time. The district court's interpretation is that a variable "must be capable of assuming, at any given time, either one of at least two values." Claim construction attached to Order of May 12, 2005, in Translogic v. Hitachi. The definitions provide some support for the examiner's position (at EA16) that a

	variable can have a constant value, e.g., when the variable in an expression is solved for a constant value. However, we adopt the district court's interpretation because it is more consistent with the dictionary definition of a quantity that may assume one of a set of values.
signal input terminal "coupled to receive" an input variable	Terminal capable of receiving an input variable. Patent owner agrees (RBr14) with the examiner's interpretation that the "input signals cannot be relied upon to patentably distinguish the claims over the combined prior art because the claims are directed to an apparatus, and the input signals are not part of this apparatus (i.e., they are merely intended use)" (EA10-11). That is, the "input variable" itself is not part of the claimed combination and these limitations are anticipated by an input terminal structure without it having to be actually connected to an input variable signal.
"having"	An open ended term, like "comprising." Therefore, the limitations defining the various stage TGM circuits do not exclude additional elements.
first, second, third, fourth, and fifth "input variables"	As noted above, patent owner agrees that the "input variables" are not part not part of the claimed structure (RBr14). However, patent owner argues that these limitations require: (1) five independent input variables; (2) that the input variables are independent from the control signal variables; and (3) the input variables cannot be constants (0 or 1). We interpret that these limitations: (1) require the signal input terminals to be "capable of" connecting to five different input variables (i.e., that there is a separate input terminal for

each variable), but that the input variables applied to the terminals do not necessarily have to be independent or different; (2) do not preclude some of the input variables from being the same as some of the control variables as long as there are separate input terminals for input variables and control signal variables; and (3) do not preclude the input signals from being constants as long as the multiplexer can accept variables.[1] A multiplexer selects one of the input variables as an output. It makes no difference to the multiplexing structure and operation whether the input variables are independent of each other or independent of the control variables, or whether the inputs are variables or constants. In any case, since the input variables are not part of the claimed structure, the nature of the input variables is not a positive claim limitation.

It also seems unlikely that patent owner would admit that a serial TGM structure which has control and input terminals capable of connecting to independent input and control variables would not infringe if it was connected so that some inputs were control variables and some inputs were constants. This goes to the use of the multiplexer structure, not the structure itself. "That which would literally infringe, if later in time, anticipates if earlier than the date of invention." Lewmar Marine, Inc. v. Barient, Inc., 827 F.2d 744, 747, 3 USPQ2d 1766, 1768 (Fed. Cir. 1987).

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[1] For example, it was noted in the patent owner's response of November 20, 2000, with respect to Japanese Laid Open Patent Application No. H1-281529, to Goto, that when an input is always a constant "1" or "0," one element of the transmission gate may usually be omitted (referring to page 7 of the translation). Such a TGM would not be capable of handling a variable.

"one of the fourth stage input terminals coupled to the third stage output terminal"	The district court interpreted this limitation as follows: "This means that the third stage output terminal cannot also be coupled to other circuitry such that the overall result is not a N:1 multiplexer circuit." Claim construction attached to Order of May 12, 2005, in Translogic v. Hitachi. However, a multiplexer structure does not cease to become a multiplexer because of the way the intermediate and/or final TGM outputs are connected to surrounding external circuitry. Therefore, we interpret this limitation to not preclude coupling the third stage output terminal to other circuitry. This difference in interpretation plays no part in the decision.
"one of the third stage input terminals coupled to the second stage output terminal"	See previous definition.
and	
"one of the second stage input terminals coupled to the first stage output terminal"	
"whereby ..."	"A 'whereby' clause that merely states the result of the limitations in the claim adds nothing to the patentability or substance of the claim." Texas Instruments, Inc. v. United States Int'l Trade Comm'n, 988 F.2d 1165, 1172, 26 USPQ2d 1018, 1023 (Fed. Cir. 1993). Here the limitations "whereby the circuit forms a 4:1" (claim 47) and "whereby the circuit forms a 5:1 multiplexer" (claim 48) merely state the result of the structure and add no further limitation. Thus, we agree with the district court's interpretation that "[t]hese clauses are to be disregarded."

Claim construction attached to Order of May 12, 2005, in Translogic v. Hitachi.

Factual findings

Scope and content of the prior art

Scope

Both Gorai and Tosser disclose serial 2-input multiplexer networks as in the claimed invention and, thus, are within the scope of the prior art. See Stratoflex, Inc. v. Aeroquip Corp., 713 F.2d 1530, 1535, 218 USPQ 871, 876 (Fed. Cir. 1983) ("The scope of the prior art has been defined as that 'reasonably pertinent to the particular problem with which the inventor was involved'."). No issue of nonanalogous art has been raised.

Content

Gorai

Gorai discusses synthesis of combinational circuits using a cascade of 2-input multiplexer units (abstract). Although multiplexers were originally developed to perform the function of mulitplexing, i.e., selecting one of several inputs to connect to a single output line, they have also found widespread application as general-purpose logic devices because it has been shown "that multiplexers (MUX) can be used as universal logic modules in the realisation of combinational circuits" (page 164). A universal logic module of a specified number of variables is a circuit that

can be used to implement <u>any</u> logic function up to that number of variables by simply arranging its input/output terminal connections. The rejection relies on the background discussion of multiplexers and the cascade (serial) arrangement of 2-input (2:1) multiplexers in sections 1 and 2, and not the method of synthesizing combinational circuits described in sections 3-8.

A conventional multiplexer with *k* inputs, *p* control lines, and one output line is shown in Fig. 1 (page 164), shown below.

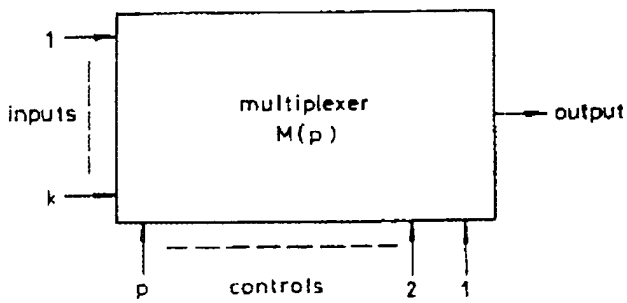


Fig. 1 *Block diagram of a multiplexer*

In a conventional multiplexer, *p* control lines select one of the $k=2^p$ inputs to output on the output line (<u>id.</u>). Gorai states that a conventional multiplexer with *p* control lines is designated as *M(p)* and "an *M(p)* can realize any function of (*p*+1) variables" (<u>id.</u>); e.g., an M(1) can realize any of the 16 possible functions of *p*+1=2 variables. It does <u>not</u> mean, as

argued by patent owner, that an *M(p)* is limited to functions of only (p+1) variables; a technical explanation is provided in Appendix A. Gorai states (id.):

> Moreover, it may be noted that a *M(p)* having $p + k$ ($= p + 2^p$) inputs has the potential of realising functions of up to ($p + 2^p$) variables. For example, let us compute the number of distinct functions realisable by *M(3)*. Since there are 11 inputs [p=3 control lines plus $k=2^3=8$ inputs], it can realise functions of up to 11 variables. By connecting three variables to three control inputs, the remaining 8 variables, or their complements or constant (0 or 1) can be connected to each of the 8 input lines. So, there are 18 possible values [8 variables, 8 variable complements, plus two constants] for connecting to each of the 8 input lines resulting in $(18)^8$ distinct functions. Some more distinct functions can be realised by interchanging the control and input variables. Thus an *M(3)* can realise more than $(18)^8$ distinct functions of which less than one part of a million forms the functions of four [p+1=3+1=4] and lower variables. The rest are the functions of 5 to 11 variables. [Explanation in brackets added.]

Thus, a 2:1 multiplexer *M(1)* with p=1 control input and $k=2^1=2$ input variables can realize functions of up to $p+2^1=3$ variables (and can realize all functions of p+1=2 variables). Each non-control input may be one of two variables, one of two variable complements, or a constant (0 or 1) (6 possible inputs) for a total of $6^2=36$ possible functions of three variables.

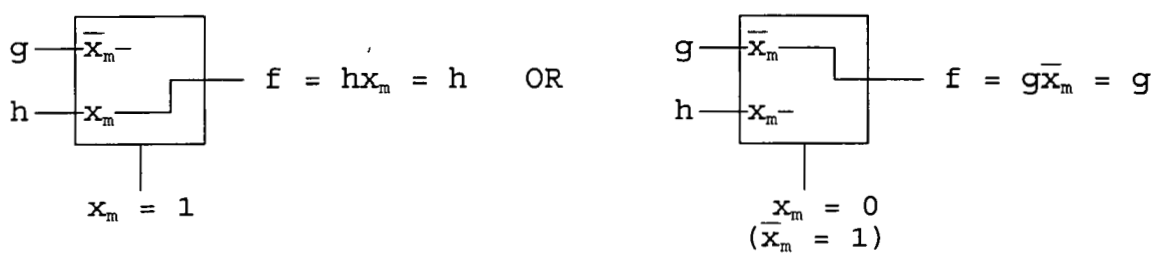
Gorai provides the general expression for an *M(1)* connected to the output of a previous *M(1)* (page 165):

> Let us consider a *M(1)* unit whose control variable is x^m [sic, x_m] and data inputs are g and h.
>
> Without loss of generality, based on Shannon's expansion theorem, the logical output f can be expressed by
>
> $$f(g,\ x_i,\ x_m) = g\bar{x}_m + h\dot{x}_m \qquad (1)$$
>
> Here g (called subfunction), is a function of binary variables (other than x_m), h can assume any one of the four values: 0, 1, x_i, or $\bar{x}_i$, where x_i is another variable other than x_m, $\dot{x}_m$ is either x_m or $\bar{x}_m$.

The symbol $\dot{x}_m$ refers to the logical state, true or inverted, of the binary variable x_m (Tosser, page 64, § 2.1); for simplicity, we refer to $\dot{x}_m$ as x_m and $\bar{x}_m$ as $\bar{x}_m$. The logical output f of a 2:1 multiplexer is a function of three variables (g, x_i, x_m) where x_m is a binary variable at the control input (page 165); input g is a function of binary variables (other than x_m) and, so, is a binary variable; and h is a binary variable x_i (other than x_m) or a constant 0 or 1).

In the function "$g\bar{x}_m + hx_m$": the "+" (sum) term represents a logical "OR" operation; the product term "$g\bar{x}_m$" (also written as "$g{\cdot}\bar{x}_m$") represents the logical "AND" of "g" and "$\bar{x}_m$"; and the product term "hx_m" (also written as "$h{\cdot}x_m$") represents the logical

AND of "h" and "x_m." That is, the function is ("g" AND "$\overline{x}_m$") OR ("h" and "x_m"). See Appendix B for a background description of logic expressions. The control variable x_m is a control signal that causes the multiplexer to select the input "*h*" as the output when x_m=1, and causes the multiplexer to select the input "*g*" as the output when x_m=0 ($\overline{x}_m$=1), as illustrated below.



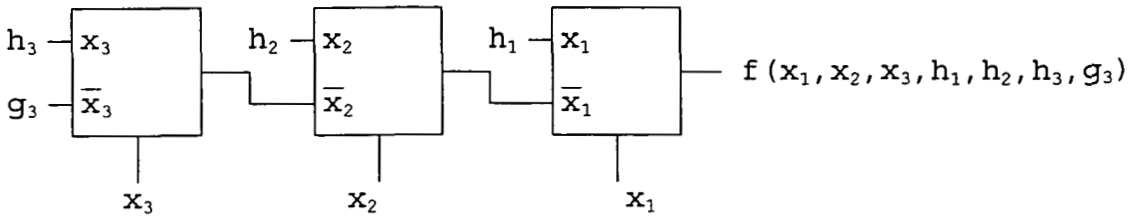
When x_m=1, the input *g* has no effect on the logic function and when x_m=0 ($\overline{x}_m$=1), the input *h* has no effect on the logic function because these inputs are not selected.

The data inputs for an *M(1)* can be connected in two ways as shown in Figs. 2a and 2b, the only difference being that x_m and $\overline{x}_m$ are interchanged in the equations.

The rejection relies on Gorai's Fig. 3, which discloses a cascade (serial) arrangement of *p*-stages of 2-input multiplexers *M(1)*. A cascade (serial) network is one in which the output

terminals of one network are directly connected to the input terminals of the other network. Each control input variable (x_1, ..., x_{p-1}, x_p) is unique and controls only one M(1). Each input variable "*h* can assume any one of the four values: 0, 1, x_i, or $\overline{x_i}$, where x_i is another variable other than x_m" (page 165). Each of the input variables (h_1, ..., h_{p-1}, h_p) can be unique, as evidenced from the previous discussion, or can be a constant or the same as a control input variable to implement a function of less than ($2p$+1) variables. Each of the subfunctions (g_1, ..., g_{p-1}, g_p) "is a function of binary variables (other than x_m)" (page 165) (e.g., g_{p-1} is a function of the binary variables g_p, h_p and x_p from the previous stage), where "[f]or the last stage, g_p is reduced to a single variable or constant 0 or 1" (page 166). Thus, for p=3, the network has three control input variables (x_1, x_2, x_3) and four data input variables (h_1, h_2, h_3, g_3), as recited in claim 47; and for p=4, the network has four control input variables (x_1, x_2, x_3, x_4) and five data input variables (h_1, h_2, h_3, h_4, g_4), as recited in claim 48.

The networks of 2:1 multiplexers in Gorai implement logic functions by appropriate selection of inputs using the control variables. For example, a general serial arrangement for p=3 in accordance with Fig. 3 is shown on the next page.



Using the multiplexer expressions in Gorai:

$$f = x_1h_1 + \bar{x}_1(x_2h_2 + \bar{x}_2(x_3h_3 + \bar{x}_3g_3))$$
$$= x_1h_1 + \bar{x}_1x_2h_2 + \bar{x}_1\bar{x}_2x_3h_3 + \bar{x}_1\bar{x}_2\bar{x}_3g_3$$

Thus, the multiplexer arrangement selects input h_1 when control variable $x_1=1$ (x_1 and x_1 are not part of the term x_1h_1 and so either can be 0 or 1) <u>OR</u> selects input h_2 when control variables $\bar{x}_1=1$ ($x_1=0$), $x_2=1$, i.e., $\bar{x}_1x_2=1$ (x_3 is not part of the term $\bar{x}_1x_2h_2$ and so can be 0 or 1) <u>OR</u> selects input h_3 when control variables $\bar{x}_1=1$ ($x_1=0$), $\bar{x}_2=1$ ($x_2=0$), $x_3=1$, i.e., $\bar{x}_1\bar{x}_2x_3=1$ <u>OR</u> selects input g_3 when control variables $\bar{x}_1=1$ ($x_1=0$), $\bar{x}_2=1$ ($x_2=0$), $\bar{x}_3=1$ ($x_3=0$), i.e., $\bar{x}_1\bar{x}_2\bar{x}_3=1$. The input selected for output is only a function of the control variables, which is, by definition, a multiplexer. <u>See also</u> Appendix C for a discussion of two examples in Gorai.

<u>Tosser</u>

Figures 6, 9, and 11 of Tosser each show a cascade of three 2-input multiplexers having 3 control inputs and 4 data inputs. It is this structure that is relied upon in the rejection. The

figures show the data inputs connected to variables (including the control variables) and constants to realize specific functions of four variables. However, the multiplexer structure does not change depending upon the inputs, and the input variables are not part of the claimed structure.

Tosser discloses a graphical method for implementing logic functions using a cascade of 2^n-input multiplexers (abstract), and, in particular, using a cascade of 2-input multiplexers (page 65, left col.). The method is valid for any function that can be represented on a Karnaugh map, i.e., with up to six variables (abstract). However, the rejection relies on the structure of a serial connection of three 2-input multiplexers, not on the method of implementing logic functions.

Weste

Weste discloses a 2:1 TGM circuit in Fig. 1.10 (page 17). "As the switches have to pass '0's and '1's equally well, complementary switches with n- and p-transistors are used. The truth table for the structure in Fig. 1.10 is shown in Table 1.4." (Pages 14 & 16). When the input to a complementary switch is "1" the input ("0" or "1") is passed to the output, and when the input to the switch is "0," the input is not defined. There is no dispute that Weste teaches a transmission gate multiplexer (TGM) as claimed.

Weste discloses using TGMs to create logic circuits (pages 172-175).[2]

Level of ordinary skill in the art

The level of ordinary skill in the art is evidenced by the references. See In re Oelrich, 579 F.2d 86, 91, 198 USPQ 210, 214 (CCPA 1978) ("the PTO usually must evaluate both the scope and content of the prior art and the level of ordinary skill solely on the cold words of the literature"); In re GPAC Inc., 57 F.3d 1573, 1579, 35 USPQ2d 1116, 1121 (Fed. Cir. 1995) (the Board did not err in adopting the approach that the level of skill in the art was best determined by the references of record); Okajima v. Bourdeau, 261 F.3d 1350, 1355, 59 USPQ2d 1795, 1797 (Fed. Cir. 2001) ("[T]he absence of specific findings on the level of skill in the art does not give rise to reversible error 'where the prior art itself reflects an appropriate level and a need for testimony is not shown.'"). Skill in the art is presumed. See In re Sovish, 769 F.2d 738, 743, 226 USPQ 771, 774 (Fed. Cir. 1985).

Based on the references, we find that one of ordinary skill in the art would have a thorough understanding of digital logic

[2] It is apparent from the truth table and multiplexer connections that "XOR" (exclusive OR) in Table 5.1 (page 174) and Fig. 5.15 (page 175) should really be "Exclusive-NOR" (XNOR).

circuits, in particular, the design of digital logic switching systems so as to be familiar with the terminology and concepts described in Gorai and Tosser, and would have sufficient skill to apply these teachings to specific problems. Such knowledge is commonly taught in an undergraduate computer science course on switching theory and logical design. One of ordinary skill in the art would also have knowledge of actual electrical implementations of multiplexers such as the transmission gate multiplexers taught in Weste. Such knowledge is commonly available in undergraduate courses in electrical engineering circuits and electronics.

Differences

Between Gorai and the subject matter of claims 47 and 48

Gorai does not disclose the implementation of the 2:1 multiplexers and, so, does not disclose using TGMs.

Between Tosser and the subject matter of claims 47 and 48

Tosser does not disclose a cascade of four 2:1 multiplexers as recited in claim 48.

Tosser does not disclose the implementation of the 2:1 multiplexers and, so, does not disclouse using TGMs.

The examples in Figs. 6, 9, and 11 of Tosser realize functions of only four variables. Nevertheless, the structure is

capable of implementing functions of seven variables and it is the cascade multiplexer structure, not the application of the cascade multiplexer structure to realize a specific function, that is relied upon. The actual variables are not part of the claimed combination and, thus, the recitations of first, second, third, and fourth input variables are not differences: it is sufficient that the structure can accept four separate input variables and three separate control variables.

Objective evidence of nonobviousness

Objective evidence of nonobviousness (also called "secondary considerations") must always be considered in making an obviousness decision, Stratoflex v. Aeroquip, 713 F.2d at 1538, 218 USPQ at 879, although it need not be necessarily conclusive on the issue of obviousness, Ashland Oil, Inc. v. Delta Resins & Refrac., Inc., 776 F.2d 281, 306, 227 USPQ 657, 674 (Fed. Cir. 1985). A "nexus" is required between the merits of the claimed invention and the evidence of secondary considerations in order for the evidence to be given substantial weight in an obviousness decision. See Stratoflex, 713 F.2d at 1539, 218 USPQ at 879. "Nexus" is a legally and factually sufficient connection between the objective evidence and the claimed invention, such that the objective evidence should be considered in the determination of nonobviousness. See Demaco Corp. v. F. Von

Langsdorff Licensing Ltd., 851 F.2d 1387, 1392, 7 USPQ2d 1222. 126 (Fed. Cir. 1988). The burden of showing nexus is on the applicant or the patent owner. See In re Huang, 100 F.3d 135, 139-140, 40 USPQ2d 1685, 1689 (Fed. Cir. 1996) ("In the ex parte process of examining a patent application, however, the PTO lacks the means or resources to gather evidence which supports or refutes the applicant's assertion that the sales constitute commercial success.").

"It is well settled 'that objective evidence or [sic, of] non-obviousness must be commensurate in scope with the claims which the evidence is offered to support.'" In re Grasselli, 713 F.2d 731, 743, 218 USPQ 769, 778 (Fed. Cir. 1983) (citing In re Tiffin, 448 F.2d 791, 792, 171 USPQ 294, 294 (CCPA 1971)). The objective evidence is not commensurate in scope (coextensive) with the claimed subject matter if the claims are broader in scope than the scope of the objective evidence, e.g., if the product included elements or features not recited in the claims which may be responsible for the commercial success or praise. See Joy Technologies Inc. v. Manbeck, 751 F. Supp. 225, 229-30, 17 USPQ2d 1257, 1259-60 (D.D.C. 1990) (and cases cited therein), aff'd, 459 F.2d 226, 22 USPQ2d 1153 (Fed. Cir. 1992); Marconi Wireless Tel. Co. v. United States, 320 U.S. 1, 35 n.20 (1943) ("Marconi's specifications disclose a large number of details of construction, none of which is claimed as invention in this

patent."); White v. Jeffrey Mining Machinery Co., 723 F.2d 1553, 1559, 220 USPQ 703, 706 (Fed. Cir. 1983) ("That Jeffrey's miner enjoyed commercial success does not support an implication that the jury found that a nexus existed between such success and the claimed invention, because the Jeffrey machine included several features not disclosed or claimed in the White patent.").

Inventor Tran's declaration

Patent owner argues that "[f]urther evidence of non-obviousness is set forth in a Statement Concerning Commercial Success and Other Objective Indicia of Non-Obviousness (attached as **Exhibit H**)" (Br22). Exhibit H refers to the Declaration Under 37 C.F.R. § 1.132 of the inventor Joseph Tran (Exhibit I to the brief) and states that "there is ample evidence of at least the commercial success that followed from this patent, as well as a suggestion of how it solved a long-felt need" (Exhibit H, page 1). Exhibit H tracks Mr. Tran's declaration and we will discuss Mr. Tran's declaration in Exhibit I rather than the unsworn statements in Exhibit H. Neither Exhibit H nor Mr. Tran's declaration discusses "long-felt need."

The examiner's position is (EA22-23):

> [T]he final arguments concerning the alleged commercial success of the invention, as set forth in the Tran declaration under 37 CFR 1.132 (after reviewing this further evidence and looking at the issue of obviousness *ab initio*,

> taking all of the prior art, arguments, etc into account), the commercial success evidence/argument does not overcome the finding [sic, conclusion] of obviousness of the claims because the required nexus is not seen to exist, i.e., mere "potential licensing", the fact that other companies may have "lauded" the invention, etc, without more, is not seen to rise to the level of "commercial success', per se. Moreover, even if such a nexus did exist, this would not be sufficient to overcome the strong motivation to use the well-known TGM circuits of Weste to implement the "black box" multiplexers of both Gorai's Fig. 3 and Tosser's Fig. 9.

We agree with the examiner that no nexus has been established between the evidence and the claimed subject matter. Mr. Tran's declaration merely sets forth a number of documents without even trying to show that what is discussed is the subject matter of claims 16 and 17 in the '666 patent (claims 47 and 48 in the reexaminations), much less trying to show a nexus. The only thing that might be considered "commercial success" is evidence of licensing to Intel Corp., which is usually treated as a separate category of objective evidence. There is no evidence of any sales of products containing the claimed subject matter that might be considered commercial success.

Mr. Tran states:

> 6. Accompanying this Declaration as Exhibit 1 is a copy of an article appearing in an on-line industry publication entitled *Silicon Strategies*, which is dated May 5, 1999, and is currently available at http://www.silicon strategies.com/sbn.news_archive/1999/19990507a10.html. This copy is true and accurate as to the content of the publication as it first appeared.

> 7. The technology covered by the claims of the '666 patent is sometimes referred to as the "M-cell technology."
>
> 8. Accompanying this declaration as Exhibit 2 is a copy of an article in *The Portland Business Journal* dated May 6, 1999. Exhibit 2 is a copy of an on-line version of the article. This copy is true and accurate as to the content of the publication as it first appeared.

The declaration merely points to the articles and does not attempt to address how the articles disclose what was actually licensed to Intel Corp. or how there is a nexus to the merits of claims 16 and 17 of the '666 patent. The article states:

> TransLogic Technology, Inc. here announced today that it has signed a five-year licensing agreement with Intel Corp., under which Intel will use TTI's computer-aided design (CAD) software tools and related technology to improve the performance of integrated circuits.

"Acquiescence by a substantial portion of the competitors in a market to the validity of a patent--generally through acceptance of a license--has been regarded as evidence supporting patentability. The theory behind use of commercial acquiescence is that persons would not usually act in a fashion contrary to their economic interests unless convinced of the patent's validity." 2 Donald S. Chisum, Patents § 5.05[3] (2003). What is said to be licensed is "computer-aided design (CAD) software tools and related technology." The '666 patent has nothing to do with CAD software tools. It is unknown what the "related technology" refers to, and we will not assume it includes or is limited to the '666 patent. Although evidence discussed infra,

indicates that the '666 patent was part of the licensing deal, we only consider the article before us. A nexus requires evidence that the licensing was due to the merits of claims 16 and 17 of the '666 patent and not to other elements and services; i.e., the objective evidence must be commensurate in scope with the claims. This article does not show what was licensed, much less any nexus to the '666 claims. It would have been easy for patent owner to provide a copy of the license agreement to show exactly what was actually licensed.

The article also states:

> TTI holds eight patents regarding IC technology. The company's patented M-cells are fully characterized transmission/pass gate programmable standard cells that help designers get the best performance from their IC designs. TTI also sells related software and a library of cells allowing customers to easily use its technology in design and development.
>
> The company's Tlogic software enables M-cells to be utilized during the logic synthesis process. By integrating Tlogic with the leading synthesis tools, IC designers will have all the benefits provided by the M-cells without having to change their current design methodology.

As written, this seems to be a description of TTI's products and company goals rather than what was actually licensed. In any case, Tlogic software has nothing to do with '666 patent, which is directed to multiplexer hardware, nor is there any evidence that "integrating Tlogic with the leading synthesis tools" was an object of the Intel licensing (this appears to refer to talks with Cadence Design Systems, Tran declaration ¶¶ 10-13).

Mr. Tran states that "[t]he technology covered by the claims of the '666 patent is sometimes referred to as the 'M-cell technology'" (¶ 7). There is no indication in the article that what was licensed was M-cell technology. Moreover, there is no evidence that "M-cell technology" is limited to claims 16 and 17 of the '666 patent. As discussed infra, there are statements that "M cell" was used by Intel to refer to the subject matter of two other TTI multiplexer patents in addition to the '666 patent. The term "cell" in "M-cell" also suggests something more than the bare multiplexer circuit. A "cell" is a small scale logic circuit for which the layout of a mask pattern for integrated circuit fabrication has already been finished (Yano et al., U.S. Patent 5,581,202, col. 1, lines 19-21, Figs. 1A & 1B, Exhibit 9 to Tran declaration). This raises the question of whether "M-cell" includes a layout pattern and mask implementation in addition to the multiplexer circuit itself. Mr. Tran's statement that "[t]he technology covered by the claims of the '666 patent is sometimes referred to as the 'M-cell technology'" (¶ 7) implies that the '666 patent claims are commensurate in scope with M-cell technology, but this has not been shown to be true and conflicts with statements that "M-cell technology" includes other patents. If M-cell technology includes additional components (design software, actual cell layouts, other kinds of multiplexer circuits, other patents, etc.) that are not part of

the '666 multiplexer claims, there is no nexus between M-cell technology and the merits of the '666 patent. We will not speculate that M-cell technology is commensurate in scope with the claims of the '666 patent or that it is what was licensed.

Exhibit 2 is a shortened version of Exhibit 1 and adds no new information.

The evidence of licensing to Intel is not entitled to any weight because it has not been established what was licensed or shown that there is a nexus between the licensing and the merits of claims 16 and 17 of the '666 patent. Mr. Tran's belief that the '666 patent was the reason for the license is not evidence.

Mr. Tran next states:

> 9. Before 1999, several key players in the integrated circuit market were introduced to TTI's M-cell technology and came to appreciate its advantages over other conventional designs.

This is merely an introductory paragraph to the next set of Exhibits. Again, it is not known what is encompassed by the term "M-cell technology."

Mr. Tran's declaration continues:

> 10. One of these players, Cadence Design Systems, is today "the world's largest supplier of electronic design technologies, methodology services, and design services" (as appearing at http://www.cadence.com/company/index.html, on September 16, 2003, copy attached as Exhibit 3). Cadence sells design synthesis tools that allow the use of TTI's Tlogic software to enable designers to use M-cells in their designs.

The first sentence is not questioned. The second sentence merely says that Cadence's design synthesis tools allow the use of TTI's Tlogic software, not that the Tlogic software was ever actually part of Cadence's design synthesis tools. The '666 patent is directed to a multiplexer structure, not design synthesis software and not the cell design.

The discussion of Cadence continues:

> 11. Cadence met with TTI to review the M-cell technology in 1993, a few months after the '666 patent was issued in December, 1992. In Cadence's internal report of the meeting, the new M-cell technology was lauded as "simple and elegant," "appealing," and offering advantages over conventional approaches:
>
> > The presentation from Translogic showed us a simple and elegant way to construct multi-level logic using CMOS inverters and N Channel transmission gates. The primary use of this technology would be the construction of a new type of cell called M cells that could replace conventional logic gates in logic synthesis and P&R. The technology is appealing in that a small number of M cells (e.g. a library of only a dozen cells) could replace a much larger library of conventional logic gates while offering smaller area and lower path delay realizations.
>
> 12. A copy of the internal Report from Jake Buurma to Jim Solomon, which is entitled "Debriefing from initial Translogic Meeting" and is dated March 26, 1993, is attached as Exhibit 4.
>
> 13. Cadence's report noted some areas where more information and development were needed, which is to be expected with developing technology, but concluded that "[i]f M cells prove effective for a wide range of logic functions and our tools can be adopted to efficiently use M cells, then we should consider adding a small library of M cells" to some of its products sold for integrated circuit design. Exhibit 4 at page 3.

There is no disclosure that the "M cells" being discussed correspond to the multiplexer structure of the '666 patent and, hence, there is no nexus. Even if it assumed that "M" stands for "multiplexer," patent owner owns U.S. Patent 5,040,139 ('139 patent), issued August 13, 1991, entitled "Transmission Gate Multiplexer (TGM) Logic Circuits and Multiplier Architectures," so there is no certainty that the discussion was limited to the '666 patent series multiplexer. The reference to "cells" implies a mask pattern layout for integrated circuit implementation, and what may have been advantageous was the cell implementation rather than the multiplexer circuit itself. In any case, the internal report simply represents impressions from a meeting and does not constitute licensing, a commitment to license, or anything that could be considered a recognized category of evidence of nonobviousness. At best, the report indicates that there was interest in "M cells" (whatever they are). Certainly, there is no evidence of sales that would constitute commercial success. The Cadence evidence is not entitled to any weight.

The declaration continues:

> 14. TTI also met with National Semiconductor in 1993. Following this meeting, an August 7, 1993 letter was sent by Thomas L. Humphrey, Director of Business Development of National Semiconductor, to Mr. Joseph Tran. A true and accurate copy of the August 17, 1993 letter is attached as Exhibit 5.
>
> 15. As expressed in Exhibit 5, National recognized TTI's then-ongoing efforts in working with Cadence to

develop design synthesis software for implementing M-cells and to test the software, expressing strong interest:

> We at National Semiconductor are definitely interested in becoming such a Beta Site. As you know National works closely with Cadence. Availability of your design methodology on Cadence tools would be a major factor in making it accessible to the National design community ....

16. As also expressed in Exhibit 5, National Semiconductor recognized TTI's proprietary rights in its innovations, noting that "should our evaluation be positive and associated costs and licensing fees be justified," National would consider adopting the technology.

The letter refers to a "proposal to Cadence to jointly develop a design automation software package that implements Translogic's design methodology" and "[a]vailability of your design methodology on Cadence tools would be a major factor in making it accessible to the National design community." Thus, the letter concerns a "design methodology," not a multiplexer hardware circuit as in the '666 patent. Moreover, the letter does not say anything about the merits of the unidentified methodology: it only states that the methodology might be adopted "should our evaluation be positive," indicating that it had not been evaluated. The letter expresses polite interest in the technology and in becoming a Beta test site if Cadence agrees to adopt TTI's design methodology. The "technology" is not identified as the series multiplexers of the '666 patent and it could be TTI's "design methodology." The letter does not constitute licensing, a commitment to license, or anything that

could be considered a recognized category of evidence of nonobviousness. Certainly, there is no evidence of sales that would constitute commercial success. The National Semiconductor evidence is not entitled to any weight.

Mr. Trans states:

> 17. TTI had also presented its M-cell technology to Hewlett Packard (HP). Following a meeting with HP, TTI received an August 3, 1993 letter from Eric Larson, ICBD Marketing Manager and Acting General Manager. A true and accurate copy of this letter is attached as Exhibit 6.
>
> 18. As indicated in Exhibit 6, HP declined an offer to work on a joint development project with TTI, but as in the case of National Semiconductor, expressed interest if design synthesis software to implement TTI's M cell technology became available:
>
>> I am encouraged to hear, however, of the negotiations with a major CAD software supplier. As we discussed, a relationship resulting in a market ready software implementing the TransLogic Design from the major CAD supplier would be a major step forward. As I understand from your business model, users would purchase software from the major CAD supplier and would obtain a license from TransLogic Design for the application of the technology in the user's products. Assuming the software cost is consistent with similar packages and the technology fee is appropriate in relation to the added value of the design improvements, the model you described could be of interest for many applications we see in ICBD.

The letter states (Exhibit 6):

> As you know, we have investigated the TransLogic Design methods and have considered the possibility of joint development of the software for our applications. We continue to be interested in the technology, however because of previous resource commitments and priorities, we are unable to work on joint development.

The subject of the letter is design "methods" and "software," whereas the '666 patent deals with multiplexer hardware, so there is no apparent nexus to the subject matter of the '666 patent claims. The letter indicates polite interest in the technology, but no identification of the technology or indication that the technology had been evaluated. The letter does not constitute licensing, a commitment to license (it states that "it is premature to make a commitment"), or anything that could be considered a recognized category of evidence of nonobviousness. There are no sales that would constitute commercial success. The Hewlett-Packard letter is not entitled to any weight in the obviousness determination.

Mr. Tran states:

> 19. Earlier, HP had requested me to synthesize two conventional HP circuits using M-cells in place of at least some typical logic gates. The M-cell modified circuits were then compared to the corresponding conventional logic gate circuits. The results were reported in an October 16, 1991 letter from Don Morris to Stan Dallas. A true and accurate copy of this letter is attached as Exhibit 7.
>
> 20. The results reported in Exhibit 7 demonstrate the advantages of the M-cell technology. The M-cell modified circuits were found to be "22% to 33% faster and 2% to 24% more dense" than the corresponding conventional logic gate circuits. Indeed, HP commented that "HP feels that these results prove that the technology has merit."
>
> 21. Stan Dallas sought confirmation of the test results in an October 23, 1991 letter to Don Morris, and Don Morris confirmed the results in his reply. A true and accurate copy of this letter with Don Morris' handwritten reply is attached as Exhibit 8.

The letter discusses that two test circuits selected by HP, and synthesized by Mr. Tran, had better performance and higher density than standard cell designs. The test circuits and how the test circuits were implemented are not described in the letter; the letter mentions a "basic logic cell," but does not identify it as a serial multiplexer circuit as claimed in claims 16 and 17 of the '666 patent (now claims 57 and 48). As of the date on the letter, October 16, 1991, Mr. Tran had the '139 patent, issued August 13, 1991, to TGM logic circuits and multiplexer architectures, and the application which matured into the '666 patent had been filed March 15, 1991, but not yet issued, so the letter might equally well refer to the '139 patent. The letter does not use the term "M-cell," but even if "M-cells" referred to the multiplexer of the '666 patent, it can be referring to the 2-stage serial multiplexer of Fig. 2, whereas the claims are directed to 3-stage and 4-stage multiplexers. Only original '666 patent claims 16, 17, 25, and 26 were limited to more than two stages, and the claims have been limited in this reexamination to 3-stage and 4-stage multiplexers because prior art disclosed the 2-stage multiplexer; see, e.g., Fig. 2 of Japanese Laid Open Patent Application H1[1989]-256219 to Goto (Goto '219 application). No nexus has been established between the contents of the letter and the 3-stage or 4-stage multiplexer subject matter of the '666 patent. The letter does not

constitute licensing, a commitment to license, or anything that could be considered a recognized category of evidence of nonobviousness. There are no sales that might constitute commercial success. The Hewlett-Packard letter is not entitled to any weight in the obviousness analysis.

> 22. As further objective indicia of nonobviousness, I point out that approximately two years after the '666 patent was granted to TTI, Hitachi filed a patent application in November 1994 that issued as U.S. Patent No. 5,581,202 (hereafter the '202 patent) to Dr. Kazuo Yano and Yasuhiku Sasaki. (Hitachi is the requesting party in this and each of the previous reexamination proceedings.) The '202 patent describes a circuit using two 2:1 multiplexers connected in series. Figure 8(b) of the patent shows 4:1 and 5:1 serial multiplexers similar to the 4:1 and 5:1 serial TGM multiplexers described in the '666 patent. During prosecution of the application that matured into the '202 patent, Hitachi represented to the U.S. Patent and Trademark Office that the circuits shown therein were patentable and not obvious. A true copy of the '202 patent is attached as Exhibit 9.
>
> 23. The subject matter of the '202 patent was further described in an article co-written by the Dr. Yano called "Lean Integration: Achieving a Quantum Leap in Performance and Cost of Logic LSIs," IEEE 1994 Custom Integrated Circuits Conference, 1994. A true copy of this article is attached as Exhibit 10.

It is not explained what category of objective evidence this evidence is supposed to fit in or how it tends to show nonobviousness of patentee's invention. The Yano '202 patent and the Yano paper do not assert that they invented the serial multiplexer. The 1994 Yano paper discloses a 2-stage TGM (the Y_1 logic cell in Fig. 1), but does not disclose a 3-stage or 4-stage TGM. Since the '666 patent discloses a 2-stage TGM (Fig. 2), and

since only claims 16, 17, 25, and 26 of the '666 patent are limited to more than two stages, it appears that patent owner considered the Yano paper to disclose the '666 invention. However, the claims have been limited in this reexamination to 3-stage and 4-stage multiplexers because prior art disclosed the 2-stage multiplexer; see, e.g., Fig. 2 of Goto '219 application. Thus, the Yano paper is not evidence of nonobviousness.

Mr. Tran's assertion that "[d]uring prosecution of the application that matured into the '202 patent, Hitachi represented to the U.S. Patent and Trademark Office that the circuits shown therein were patentable and not obvious" (¶ 22) is not supported by evidence from the prosecution history showing that it was represented that the circuits of Fig. 8B were patentable. Applicants do not assert that everything in the specification and drawings is novel and nonobvious: applicants only assert that the claimed invention is patentable over prior art known to them. The claims of the '202 patent are not directed to the '666 multiplexer circuits. There is no evidence of copying. The Yano '202 patent and the Yano paper are not entitled to any weight in the obviousness analysis.

Supplemental court documents

On May 19, 2005, patent owner filed an Information Disclosure Statement (IDS) under 37 C.F.R. §§ 1.555 and 1.98 providing a copy of numerous court documents from Translogic v. Hitachi, including: (1) transcripts from jury trial on damages (Vols. 1A, 1B, 2A, 2B, 3A, 3B, and 4A); (2) order of February 22, 2005, granting plaintiff's motion for summary judgment of infringement; (3) Hitachi's Emergency Motion for Stay of Permanent Injunction dated May 12, 2005; (3) district court order granting permanent injunction entered May 12, 2005; (4) verdict form (finding inducement of infringement and awarding $86.5 million in damages for infringement); (5) transcript of verdict proceedings of May 6, 2005; (6) Welcome to the family - the SuperH RISC Engine Family of 32-bit RISC Microcomputers, HITACHI Today, Vol. 38 (Winter 1997); (7) HITACHI Technology PARTNER, Design Solutions from Hitachi Semiconductor (America) Inc. (July/August 1998); and (8) Civil Docket for Case #: 3:99-cv-00407-PA, Translogic Technology, Inc. v. Hitachi, Ltd. et al., U.S. District Court, District of Oregon (Portland). Patent owner asserted that "[c]ertain of these documents pertain directly to objective indicia of non-obviousness including commercial success, licensing, and copying of the invention as claimed in the pending merged reexaminations," referring to

licensing by Intel Corp. and the commercial success and widespread use of products incorporating the claimed invention.

At the oral hearing on May 31, 2005, this panel gave the patent owner one week to file a paper describing how the various documents evidenced nonobviousness. We indicated that the panel would exercise our discretion in deciding whether to consider this new evidence. Patent owner timely filed a statement on June 6, 2005 (pages referred to as "S__").

The purpose of an IDS in a reexamination proceeding is to satisfy the duty of the individuals associated with the patent owner to disclose to the Office all information known to be material to patentability. See 37 C.F.R. § 1.555(a). That is, an IDS presents evidence which bears on the issue of unpatentability, not patentability. Because all of the claims stand rejected, there is no reason to remand the case to the examiner for consideration of the IDS. The reexamination proceedings have already gone on long enough. Although we are not required to consider patent owner's statement, we nonetheless do so because a patent is involved. We address only the arguments actually presented by patent owner. Cf. In re Baxter Travenol Labs., 952 F.2d 388, 391, 21 USPQ2d 1281, 1285 (Fed. Cir. 1991) ("It is not the function of this court to examine the claims in greater detail than argued by an appellant, looking for nonobvious distinctions over the prior art."). Patent owner is

precluded from raising new arguments on appeal. See In re Watts, 354 F.3d 1362, 1367, 69 USPQ2d 1453, 1457 (Fed. Cir. 2004) ("Just as it is important that the PTO in general be barred from raising new arguments on appeal to justify or support a decision of the Board, it is important that the applicant challenging a decision not be permitted to raise arguments on appeal that were not presented to the Board." (Footnote omitted.)).

Patent owner states in the introductory paragraph (S1-2):

> These itemized portions pertain to objective indicia such as licensing, initial skepticism and praise, commercial success, and copying of the claimed invention. As used herein, any products designated as "infringing" were found to infringe original claims 16 and 17 that remain pending (but are renumbered) in the merged reexaminations. The portions designated below in combination with other materials such as, for example, Mr. Tran's Declaration Concerning Commercial Success, establish that the invention of claims 16 and 17 provides results that are surprising to those of skill in the art, was praised by those of skill in the art by, for example being licensed for use in the Pentium 4 processor, and has demonstrated commercial success in a variety of products.

The items are listed in the statement with no explanation of how they fit into a category of evidence of nonobviousness or how there is a nexus to the merits of the claimed invention, e.g., "Statement by Mr. Axelrod [attorney for Hitachi] that all Hitachi SH-4 products include infringing circuit segments (at 46)" (S2) and "Testimony by Mr. Tran concerning software needed for automated inclusion of patented multiplexer circuits (at 8)" (S2). Patent owner essentially leaves it to us to do the

analysis for it. For this reason alone, the statement is unpersuasive. Nevertheless, we have tried to determine how the various statements might be considered to be evidence of nonobviousness.

Although patent owner refers to "initial skepticism" we find no statements which might fall into this category. Although patent owner refers to "copying of the claimed invention," none of the statements deals with "copying." It was asserted by defendants in the district court that there was no evidence of copying because the creation of circuits that give rise to claims in dispute were almost always by EDA (Electronic Design Automation) synthesis software (opening statement by Mr. Axelrod, attorney for defendant Hitachi, Vol. 1A, p. 55, lines 13-22; testimony of Mr. Hattori, Vol. 2B, p. 110, line 21, to p. 111, line 9). As far as we can determine, there is no evidence of copying. In any case, "more than the mere fact of copying by an accused infringer is needed to make that action significant to a determination of the obviousness issue." Cable Electric Products, Inc. v. Genmark, Inc., 770 F.2d 1015, 1028, 226 USPQ 881, 889 (Fed. Cir. 1985). "[Copying] may have occurred out of contempt for the specific patent in question." Id. There is no doubt in this case that Hitachi considered the '666 patent to be invalid.

The statements break down into four categories: (1) commercial success of defendant Hitachi's processors; (2) licensing to Intel; (3) performance of the '666 circuits and statements about Dr. Yano's paper and '202 patent; and (4) statements by Intel about TTI technology.

(1)

The "commercial success of products incorporating the claimed invention" (S5) relied upon by patent owner is the commercial success of Hitachi's SH-3 and SH-4 series microprocessors, which includes circuit segments which were found to infringe '666 patent claims 16 and 17 (rewritten here as claims 47 and 48) and which are incorporated in products by SnapGear, Compaq, Medtronic, Sega of America, Casio, Inc., LexMark, and others (S2-4). The argued commercial success is <u>not</u> due to any product by the patent owner. It is stated that "Intel licensed the patented technology for use in one of the most important products ever introduced, the Pentium 4" (S2). However, TTI's technology was never used in the Pentium 4 and the Pentium 4's success does not count as commercial success. It is stated that $62 million is the approximate total value of U.S. sales of infringing Hitachi products (S3). References to infringement, use of patented technology, and the amount of Hitachi sales of infringing products fall into this category.

Commercial success of an infringer's success and success of others may be entitled to weight. See 2 Patents § 5.05[2][g]. However, patent owner has not even attempted to establish a nexus between the commercial success of Hitachi's microprocessors and the merits of the claimed invention. The SH3 and SH-4 series microprocessors are complex, high-performance RISC (reduced instruction set computer) microprocessors verified to be compatible with the Windows CE operating system and designed to offer low power consumption and to be used with a wide range of multimedia and communication products; see HITACHI Technology PARTNER under News Briefs and HITACHI Today. Testimony indicates that the infringing circuit segments formed an extremely small fraction of the overall microprocessors. For example, the percentage of transistors in the infringing circuits in the 7705 SH-3 (SH7705) microprocessor of the 5.2 million total number of transistors was 0.0064 percent (Vol. 2B, p. 112, lines 1-14) and the percentages of transistors in the infringing circuits to the total number of transistors in the 7750 SH-4 (SH7750) and 7760 SH-4 (SH7760) processors were 0.0056 percent and 0.0019 percent, respectively (Vol. 2B, p. 112, line 15, to p. 113, line 6). There were about 184 transistors in the infringing circuits and the SH7750 has about 3.3 million transistors and the SH7760 has almost 10 million transistors (opening statement of Mr. Axelrod, Vol. 1A, p. 46, line 22, to p. 47, line 3). There is no showing

whatsoever that the success of the Hitachi microprocessors, and the products that they were part of, were due, even in part, to the merits of the '666 patent. In addition to failing to show that the commercial success was not due to unclaimed features of the operation of the 99.99% of the transistors in the microprocessors, patent owner has failed to address all the usual reasons why commercial success may not demonstrate a nexus to the merits of the claimed invention, such as advertising, seller's dominant market position, etc. Accordingly, no nexus has been established. The evidence of commercial success of Hitachi's microprocessors and of the products that they were part of is not entitled to any weight in the obviousness determination.

(2)

The terms of the Intel license from TTI are not complete. The total value of the deal was $5 million and involved TTI patents, 5,040,139, 5,162,666, and 5,200,907 (testimony by Mr. Tran, Vol. 1B, p. 53, line 2, to p. 54, line 12). The deal was for $5 million over five years (testimony by Mr. Tran, Vol. 1B, p. 59, line 20). Intel internally assigned a value of $3.5 million to the three patents (testimony by Mr. Napper, witness for defendant, Vol. 3B, p. 6, lines 16-19). As stated in

the opening statement by Mr. Axelrod, Vol. 1A, p. 61, line 9, to p. 62, line 17):

> What Intel negotiated for and got were 25 licenses to the software that Translogic developed. That includes the library products that you'll hear testimony about. This software and this library is basically the work product or end result of what it was that Translogic had been developing with many, many dollars of investors' money over a number of years.
>
> Then they got support, maintenance and upgrades to that software capability from Intel for over a period of five years. Mr. Tran will testify about what that support involved. He has testified previously sometimes it involved his entire company coming to work - not coming to work but supporting Intel or working on a particular problem Intel may have. So it was not an insignificant commitment.
>
> Then you will see in the course of their negotiations Intel insisted that it get license rights to all three of the patents, very different patents, that use this transmission gate technology that Intel was interested in and thought it might use in connection with the Pentium 4 product that was going to be coming out.
>
> So it got rights to all three patents. I think they refer to them in the Intel license as the M cell patents. Then it got a release of any of the claims that Translogic may have had that Intel had done something in the past that infringed. You have this bundle as one reference point, and you kind of have to sort out through that.
>
> The parties will give you very conflicting views. I think Mr. Love indicated they will want to say: Well that was all given to them for free, and the only thing that counted was the '666 patent, and we even discounted that. That's one of the things that you will be asked to evaluate.

<u>See also</u> Testimony of Mr. Scanlon (Vol. 2A, p. 94, line 17, to p. 96, line 21); closing arguments of Mr. Elkins, Vol. 3B, p. 115, line 18, to p. 117, line 19). Thus, the license apparently included many components in addition to the

multiplexer circuit of the '666 patent. Although Mr. Tran testifies that it is his opinion that the main value is in the '666 patent (Vol. 1B, p. 54, lin 18, to p. 56, line 4), we find no evidence that Intel considered the '666 patent to be the main reason for the license. Patent owner could have, but did not provide a copy of the license agreement so that it could be evaluated. The license agreement could clarify the meaning of the term "M cell," which Mr. Tran uses to refer to the '666 patent, but which was apparently used by Intel to refer to all three patents. No nexus has been established between the Intel licensing agreement and the merits of the '666 patent and the licensing agreement is not entitled to any weight.

Moreover, Intel took a license after TTI had discussions with Hitachi and was considering suing Hitachi for infringement. Intel apparently considered licensing TTI's patents to avoid litigation costs. See Question by Mr. Elkins, attorney for defendants, on cross-examination (Vol. 2A, p. 100, lines 17-20: "[P]age 5 of Exhibit 266 ... indicates that Intel apparently saw the benefit to taking a license because it would mitigate patent infringement risks." "[Licensing programs] are not infallible guides to patentability. They sometimes succeed because they are mutually beneficial to the licensed group or because of business judgments that it is cheaper to take licenses than to defend infringement suits, or for other reasons unrelated to the

unobviousness of the licensed subject matter." EWP Corp. v. Reliance Universal Inc., 755 F.2d 898, 907-908, 225 USPQ 20, 26 (Fed. Cir. 1985). Intel could have decided that it was cheaper to take a license to all of TTI's patents than to get involved in an infringement suit. Thus, no nexus has been established between the Intel license agreement and the merits of the '666 patent, and the license agreement is not entitled to any weight in the obviousness determination.

(3)

Several items deal with test results from tests run by Intel and Hewlett-Packard (testimony by Mr. Tran, Vol. 1A, pp. 81-83; Vol. 1B, pp. 3-9). Patent owner has not provided any copies of the test results and there is no way of telling what was tested or what it was compared against or what the results were. The testimony of Mr. Tran is not clear as to exactly what was tested or what was superior in the test results. Some of the testimony indicates that the results were dependent on Mr. Tran's implementation of the multiplexer; e.g., "I need to design it, to lay it out, to extract it, to characterize test it -- after that, the real testing data that it produced, to see that the result of the testing, how fast the multiplexer would be in the real condition of the process that Intel have at that time" (testimony by Mr, Tran, Vol. 1A, p. 82, lines 5-10). We will not speculate on what was actually tested or what the test results show; the

tests might just show measured results with no conclusion of whether the results are ordinary or unexpectedly good. Patent owner could have provided actual copies of the tests. The testimony of Mr. Tran referred to in the statement concerning the testing by Intel and Hewlett-Packard does not prove a nexus to the claimed invention and is not entitled to any weight.

The statement also refers to "Testimony by Mr. Tran concerning promotion of serial multiplexer technology, referred to as Y-cell technology, in Hitachi premier product (SH-4), praise for remarkable speed improvement obtainable with serial multiplexer technology as noted by Mr. Yano's '202 patent, and statement that increased speed is available with a power reduction of 23% ([Vol. 1B] at 10-18)" (S2). These statements appear to be just Mr. Tran's personal interpretation of the facts. While the SH-4 series microprocessors were found to contain 4:1 and 5:1 serial multiplexers under the '666 patent, there is no evidence that Hitachi "promoted" serial multiplexer technology or that it even knew that it contained this circuitry. It is true that the Yano '202 patent shows 4:1 and 5:1 serial multiplexers in Fig. 8B, but this is not Yano's claimed invention; the figure shows many ways to arrange multiplexer circuits, none of which was claimed. Mr. Tran's testimony does not demonstrate a nexus between the Yano patent and article and

the merits of the claims 16 and 17 of the '666 patent and is not entitled to any weight in the obviousness determination.

(4)

The statement refers to statements by Mr. Love, one of TTI's attorneys, referencing an Intel document that states: "Reduces interconnects and improves performance of RLS. Provides faster, denser, lower-power synthesized logic. Is target for deployment in Northwood." (Vol. 3B, p. 103, lines 13-15.) We do not have a copy of this document and do not know the context of the statement. Perhaps the statement refers to all three TTI patents, which deal with multiplexers. These statements, in isolation, provide no nexus to the merits of the '666 patent.

The statement also refers to a "Statement by Mr. Love referencing an Intel statement concerning lack of alternatives to patented technology ('There's no substitute at this time.') ([Vol. 3B] at 107)" (S4). The full quotation is "Don't use TTI technology. There's no substitute at this time." (Vol. 3B, p. 107, lines 7-8.) It is ambiguous whether this means there are no alternatives to TTI's technology or that Intel was not planning to substitute TTI's technology in their product. We do not have a copy of this document and we do not know the context of the statement. This Intel statement, in isolation, provides no nexus to the merits of the '666 patent. Accordingly, the

statements of Mr. Love are not entitled to weight in the obviousness determination.

Conclusion regarding objective evidence

For the reasons discussed above, we find that no nexus has been established between the evidence and the merits of claims 16 and 17 of the '666 patent (now claims 47 and 48). The evidence is not entitled to any weight in the obviousness determination.

Motivation

Whether there is motivation to combine the references is a question of fact drawing on the factors of Graham v. John Deere Co., 383 U.S. 1, 17-18, 148 USPQ 459, 467 (1966). See McGinley v. Franklin Sports, Inc., 262 F.3d 1339, 1351-52, 60 USPQ2d 1001, 1008 (Fed. Cir. 2001). This is a fifth factual finding.

The networks in Gorai and Tosser are only block diagrams and must be implemented with actual, physical circuits to be useful. One of ordinary skill in the art would have recognized that any known 2:1 multiplexer circuit could be used to implement the 2:1 multiplexers in Gorai and Tosser. Weste teaches that 2:1 TGM circuits were well known in the logic design art. The motivation to combine flows from the fact that physical circuits are needed to implement the multiplexer blocks in Gorai and Tosser, and

because TGM circuits were a well-known multiplexer implementation to those of ordinary skill in the art as taught by Weste.

Obviousness conclusion

One of ordinary skill in the art at the time of the invention would have been motivated to use 2:1 transmission gate multiplexers (TGMs) as taught by Weste for the 2:1 multiplexers in the series arrangements of multiplexers in Gorai and Tosser because one skilled in the art would appreciated that any conventional multiplexer circuit could be utilized to implement the 2:1 multiplexer blocks in Gorai and Tosser, and because TGMs were well-known multiplexer circuits as evidenced by Weste. We determined that the objective evidence of nonobviousness is not entitled to any weight in the obviousness determination because no nexus has been shown to the merits of the subject matter of claims 16 and 17 of the '666 patent (claims 47 and 48 in these reexaminations). Nevertheless, even if the evidence was somehow related to the merits of the '666 patent, it would not overcome the very strong case of obviousness. The evidence does not show that TGMs would have been a nonobvious multiplexer implementation.

Arguments

Patent owner's arguments were considered in making the obviousness determination, but were not convincing for the following reasons.

(1)

Patent owner argues that a *p*-stage Gorai circuit can receive only (*p*+1) variables (*p* control variables plus 1 input variable) and, therefore, the 7 input terminals of a 3-stage Gorai circuit is configured to realize a function of only 4 different variables instead of 7 variables as claimed (Br14-15; RBr6-8). It is argued that in the general *p*-stage multiplexer network arrangement of Fig. 3, the control inputs (x_1, ..., x_{p-1}, x_p) and the g_p input are variables, but the h_k inputs must be a constant (0 or 1) or one of the variables (x_1, ..., x_{p-1}, x_p, g_p) (Br15).

This argument is based on the statement in Gorai that "an *M(p)* can realise any function of (*p*+1) variables" (page 164) and is incorrect for several reasons. First, the statement means that all possible functions of (*p*+1) variables can be realized, not that only functions of (*p*+1) variables can be realized; see Appendix A for a technical explanation. Second, Gorai discloses that "an *M(p)* having $p + k$ (= $p + 2^p$) inputs has the potential of realising functions of up to ($p + 2^p$) variables" (page 164), so

an M(p) is clearly not limited to functions of (p+1) variables. A 2:1 multiplexer (p=1, 2^p=2) can realize functions of up to three variables: one control variable and two input variables. Third, Gorai discloses that for each stage the data input "h can assume any one of the four values: 0, 1, x_i or $\overline{x_I}$, where x_i is another variable other than x_m [the control variable for that stage]" (page 165). The input variable x_i is not required to be, but can be, a function of one of the control variables x_m. Fourth, the statement about $M(p)$ does not apply to a cascade of 2:1 multiplexers: an $M(p)$ is a conventional multiplexer with p control lines to select one of $k=2^p$ inputs to output on the output line. Because each input to a multiplexer can be a different variable, the cascade circuit in Fig. 3 can accept (2p+1) different variables (p control variables and (p+1) input variables); thus, a 3-stage network would have three control variables and four input variables as recited in claim 47, and a 4-stage network would have four control variables and five input variables as recited in claim 48.

(2)

It is argued that the examples in Gorai and Tosser lack the requisite number of input terminals for control and input variables to perform a multiplexing function.

Gorai

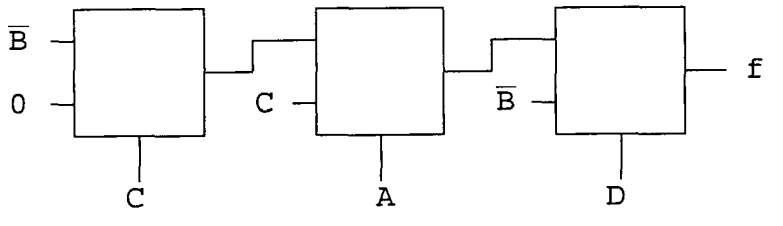
It is argued that the combinational circuits in the examples in Figs. 6, 8, 9, and 10 of Gorai "all fail to show or include three cascaded 2:1 multiplexers coupled to receive seven variables (four input variables and three control signals) or nine variables (five input variables and four control signals) as recited in the pending claims" (RBr7).

To keep the analysis simple, the rejection over Gorai relies on the general *p*-stage cascade multiplexer circuit taught in Gorai's Fig. 3 and the corresponding text. This cascade multiplexer arrangement has inputs for *p* control variables and (*p*+1) input variables. Thus, a 3-stage multiplexer has inputs for three control variables and four different input variables, as recited in claim 47, and a 4-stage multiplexer has inputs for four control variables and five different input variables, as recited in claim 48. The fact that the examples apply this multiplexer structure to realize functions of only four variables does not change the multiplexer structure.

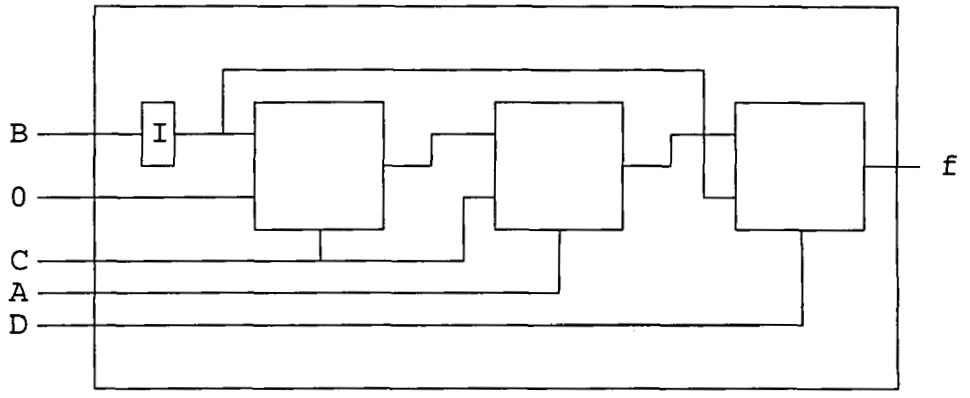
Tosser

It is argued that the circuit in Fig. 9 of Tosser, relied upon by the examiner, is only coupled to receive two different input variables, D (or $\overline{D}$) and C, where "0" is a constant (Br12-13), and "a circuit coupled to receive only two input variables cannot be a 4:1 multiplexer that must necessarily be coupled to receive four different input variables in order to select one of the four different input variables as an output" (Br13). It is argued that Fig. 9 discloses coupling the same variable (C or $\overline{C}$) to both a control input terminal and a signal input terminal and, "[b]ecause Tosser's Fig. 9 circuit does not distinguish input variables and control signals, Tosser's Fig. 9 circuit cannot perform a 4:1 multiplexing function" (Br16).

Patent owner also argues that Tosser's Fig. 6 does not show a 4:1 serial multiplexer. Figure 6 of Tosser is shown below.



Patent owner presents the following figure adapted from Tosser's Fig. 6:



I = inverter

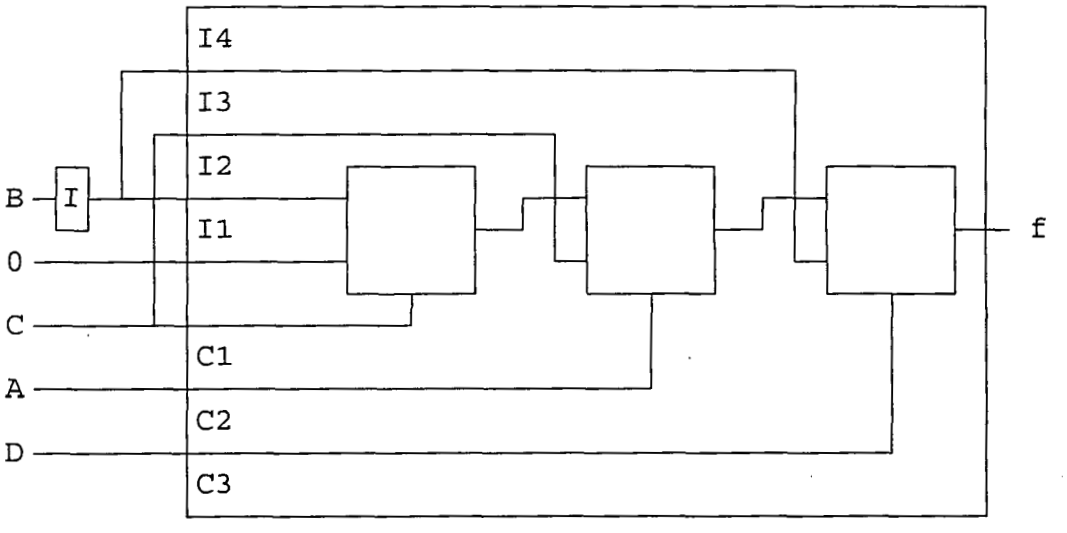
It is argued (Br16):

> This circuit is configured to receive at most four input variables (*A*,*B*,*C*,*D*). One input (*C*) is coupled to a control input of the first stage and to a signal input of the second stage. Thus, this three stage cascade also lacks any distinction of control signals and input variables as recited in the subject claims. In addition, only two inputs (*B*,*C*) are coupled to signal input terminals, and only these two inputs can be coupled to the output. Inputs (*A*,*D*) are coupled only to control inputs and cannot be selected for coupling to the output. Thus, this circuit cannot perform the multiplexing function of the claimed 4:1 serial multiplexer circuits.

It is argued that expert opinion reinforces the conclusion that the circuit of Tosser's Fig. 6 is not a multiplexer (Br17). Dr. Sechen is a witness adverse to the patent owner in the related litigation (Br17). Figure 1 of Exhibit 14 of Dr. Sechen's deposition (Exhibit G to the brief) shows the same

figure adapted from Tosser's Fig. 6 above. Dr. Sechen stated that "that circuit is certainly not a serial multiplexer." Deposition of Carl Sechen, Ph.D., August 18, 2003, at 161 (Exhibit G to brief). It is argued that "[m]ultiplexer circuits necessarily have terminals for control signals and distinct terminals for input variables" (Br17).

Patent owner's graphical arguments concerning Fig. 6 also apply to Fig. 9. We prefer to redraw Fig. 6 as shown below.



I = inverter

The structure of three multiplexers in series with three control variables (C1,C2,C3) and four input variables (I1,I2,I3,I4) is clearly present. Claim 47 reads on this structure (except for the TGMs) because it does not preclude the

additional structure Tosser uses to implement the logic function, and because the actual inputs are not part of the claim. That is, claim 47 is directed to the bare multiplexer circuit, whereas Tosser shows the same multiplexer circuit (except for the TGMs) with the inputs connected to realize a specific logic function. The examples in Gorai also show serial multiplexer structures, as claimed (except for the TGMs), connected to realize specific logic functions.

(3)

It is argued that Gorai and Tosser do not teach that the input variables and control variables are independent of each other. It is argued that coupling an input terminal and a control terminal to receive the same variable, as in Fig. 9 of Tosser, which are coupled to receive $\overline{C}$ and C, respectively, is "forbidden in a multiplexer circuit" (RBr12) and "[i]n the claimed multiplexer circuits, input variables are never applied to control input terminals, and control input signals are never applied to input terminals, and can never appear as outputs" (RBr12). Patent owner argues (RBr17) that the examiner errs in stating that "nowhere do the claims recite that the input variables are independent of each other, or that they are independent of the control inputs" (EA14-15). It is argued that the input variables are distinguished as first, second, third, and fourth input variables, the control signals are distinguished

as first, second, and third control signals and "all variables have different names, indicating they are different" (RBr17).

As noted in the claim interpretation section, the variables are not part of the claims, which are directed to a multiplexer structure, not how it is used. Thus, it is sufficient that the input terminals are "capable of" being connected to independent control and input variables. Claim 47 does <u>not</u> require the first, second, third, and fourth input variables to be different variables from the control variables. It is <u>not</u> forbidden for a multiplexer to have some of the input variables set to be the same as some of the control variables. A multiplexer selects one of the input variables as an output. It makes no difference to the multiplexer structure whether the input variables are independent of each other or of the control variables, or whether the inputs are variables or constants; it is still a structure that selects one of the inputs to be output.

Nevertheless, Fig. 3 and the corresponding text of Gorai teaches that the input and control variables can all be independent. The structure of a 3-stage series of multiplexers can be connected to realize functions of seven or fewer variables without any change in the multiplexer structure itself.

Tosser shows a multiplexer structure as claimed (except for the use of TGMs) which is connected in certain ways to realize functions of four variables. The fact that the multiplexer is

applied to realize functions of only four variables does not alter the fact that the structure could be connected to realize functions of seven variables.

(4)

It is argued that Gorai and Tosser teach combinational logic circuits, not multiplexer circuits. It is argued (RBr5):

> Gorai teaches a specific way to cascade 2:1 multiplexer circuits to form combinational logic circuits in which inputs are combined to realize a logical function. In contrast, the pending claims are directed to multiplexer circuits in which one of a plurality of inputs is selected for delivery to an output, but in which no inputs are combined.

And (RBr9):

> Tosser, like Gorai, teaches a specific way to cascade multiplexer circuits to implement logic functions. In contrast, the pending claims are directed to multiplexer circuits in which one of a plurality of inputs is delivered to an output, not circuits that realize combinational logic.

Patent owner argues that the examiner errs in concluding (at EA16) that the combinational logic circuits of Gorai's Fig. 3 and Tosser's Fig. 9 are clearly performing a multiplexer function and in concluding that any circuit that includes a 2:1 multiplexer is a multiplexer regardless of the coupling of its inputs and outputs (RBr18). It is argued that under this interpretation, the buffer, NAND gate, and flip-flop illustrated in Exhibit D to the reply brief would become multiplexers, which is an unreasonable construction (RBr18). It is argued that a "multiplexer" is defined as "a hardware circuit for selecting a

single output from multiple inputs," and that the circuits in Gorai and Tosser do not perform a multiplexer function (RBr18).

These arguments are totally without merit. Gorai teaches that "multiplexers (MUX) can be used as universal logic modules in the realisation of combinational circuits" (page 164). A multiplexer or a series of multiplexers can be utilized to implement combinational logic circuits, such as buffers and NAND circuits and more complicated functions, by selecting a single output from multiple inputs according to the control variables. For example, as noted in Appendix A, there are 16 logic functions of two variables that may be implemented with a 2:1 multiplexer (not all of which are useful), including AND, NAND, OR, and buffer functions. Multiplexers remain multiplexers no matter what logic circuit they implement by different connections of the inputs. The claimed multiplexers will inherently realize combinational logic functions when they are connected to receive specific combinations of variables as patent owner is well aware. U.S. Patent 5,040,139 to Dzung J. Tran, the same inventor as the '666 patent, and also assigned to patent owner, shows the use of multiplexers to realize logic functions. And, if the discussions between TTI and Cadence involved the '666 patent's multiplexer, the primary use was to construct multi-level logic (Exhibit 4 to Tran declaration of Exhibit I).

(5)

It is argued that Gorai and Tosser teach using conventional binary tree multiplexers in their combinational logic circuits and do not suggest the claimed serial multiplexer circuits (Br19). It is argued that "[b]oth Tosser and Gorai turn to conventional [binary tree] multiplexer circuits whenever an N:1 multiplexer circuit is needed" (emphasis omitted) (Br19).

Apparently the argument is that Gorai and Tosser do not call a cascade arrangement of multiplexers a "multiplexer," so it must not be a multiplexer and the only multiplexers are the individual multiplexers that make up the network. Since Gorai and Tosser disclose a serial network of 2:1 multiplexers, the same structure as patent owner's invention, it is not known how patent owner can reasonably make this argument. The fact that a multiplexer structure can be connected in various ways to implement different logic functions does not mean that it is not a multiplexer.

(6)

It is argued that one skilled in the art would not arrive at the claimed 4:1 or 5:1 multiplexer circuits by following Gorai's synthesis method of generating a minterm table and applying an algorithm to the table. It is argued (RBr8-9):

> Because Gorai does not teach or suggest a minterm table for a serial multiplexer function, and provides no motivation to obtain such a minterm table or ratio parameters for a serial multiplexing function, Gorai necessarily fails to teach or suggest any such serial multiplexer circuits. Moreover,

> even if Gorai taught or suggested an appropriate minterm table, following Gorai's teaching of minterm table (ratio parameters) + algorithm = cascade circuit, would not produce the claimed multiplexer circuits. As stated in the Declaration of Joseph Tran (attached as Exhibit C [to the reply brief], submitted on September 17, 2003), following Gorai's procedure would produce a 4:1 multiplexer having six stages and a 5:1 multiplexer circuit having eight stages, not three or four stages recited in the pending claims. Therefore, using the method of Gorai to construct a multiplexer circuit having a truth table that is identical to that of the claimed 4:1 multiplexer circuits fails to produce the claimed multiplexer circuit.

The rejection does not rely on following Gorai's synthesis method. There is no need to follow Gorai's synthesis method to realize a 4:1 or 5:1 multiplexer because Fig. 3 already shows a the *p*-stage serial multiplexer circuit which is a (*p*+1):1 multiplexer.

(7)

Patent owner notes that the rejections of the 5:1 multiplexer claims appear to be based on a combination of Tosser modified to include an additional (fourth) stage and Weste (RBr19). It is argued that "even if Tosser disclosed 4:1 multiplexer circuits, Tosser expressly states that his method cannot be extended, and teaches away from providing a fourth stage such as recited in the 5:1 multiplexer circuit claims" (RBr19-20), so the "5:1 multiplexer circuit claims are separately patentable over the Tosser/Weste combination" (RBr20).

It is true that Tosser only expressly shows three multiplexer stages. Nevertheless, Tosser does not state that a cascade of multiplexers is limited to three stages; it only states that the synthesis method is limited to functions of six variables. The examiner concluded that one of ordinary skill in the art would have been motivated to extend the teaching of three stages of 2:1 multiplexers in Tosser to four stages to allow processing of more input signals (FR7) and patent owner has not shown any error in this reasoning. The rejection relies on the multiplexer structure shown in the figures, not on Tosser's method of synthesizing a logic circuit.

(8)

Patent owner argues that there is no motivation to combine the teachings of Gorai or Tosser with Weste's TGM circuit (Br21-22). It is argued that Weste teaches that CMOS transistor pairs should be avoided in serial connections such as those recited in the pending claims because, "[a]ccording to Weste [at pages 174-175], pass transistor networks such as TGMs incur extra delays, exhibit higher internal node capacitances and higher series resistances, consume more circuit area, and require true and complement control variables" (Br22).

Weste discloses that pass transistor logic is popular in nMOS circuits and "the simplest example probably being a 2-input multiplexer" (page 172). Weste discloses (pages 174-175):

> The apparent advantages of pass transistor networks in CMOS should be studied carefully and judiciously utilized. A few points detract from the use of pass networks. To achieve good logic levels complementary pass networks are desirable but incur extra delay in pull-down. In comparison to regular gates, the merging of source and drain regions is difficult, leading to higher internal node capacitances. Finally true and complement control variables are required.

Thus, Weste disclose that pass transistor (transmission gate) networks have advantages and a few disadvantages. One skilled in the art would have been motivated to use TGMs for their known advantages and there is nothing that would lead one skilled in the art away from using TGMs.

Weste does not state that TGMs exhibit higher series resistances and consume more circuit area, as argued by patent owner. Patent owner is probably relying on the article by C. Zhang, Universal logic gate transmission gate array, Electronic Engineering, October 1985, pages 61-67, at page 63, which mentions these disadvantages for one circuit embodiment. Nevertheless, Zhang discloses that other circuits can overcome these problems. In any case, both Weste and Zhang disclose that TGMs are used for multiplexer circuits. Therefore, the advantages must outweigh whatever disadvantages TGMs might have, and one of ordinary skill in the art would not have been lead

away from using TGMs; see EA21-22. Patent owner does not claim to have overcome the disadvantages of TGMs.

(9)

Patent owner argues that "[f]urther evidence of non-obviousness is set forth in a Statement Concerning Commercial Success and Other Objective Indicia of Non-Obviousness" (Br22).

This statement has been considered in the discussion of the objective evidence.

(10)

Patent owner argues that the examiner errs in stating (at EA14) that a variable and its logical complement, e.g., D and $\overline{D}$, are two different variables (RBr15-16).

We agree with patent owner that a variable and its logical complement are the same variable. A variable and its complement represent different states of the same variable. However, the examiner's statement does not affect the decision. Gorai teaches that a p-stage serial arrangement of 2:1 multiplexers can receive p control variables and (p+1) input variables. The examples in Tosser and Gorai disclose a serial arrangement of three 2:1 multiplexers, which forms a multiplexer that meets the limitations of claim 47 (except for the TGMs). The fact that the examples show the multiplexer arrangement connected in specific ways to realize specific functions of less than the number of

variables that could be handled is not important because: (1) the claims are open ended and do not preclude the additional structure that is used to connect the input terminals of the multiplexers to specific variables; and (2) the input variables are not part of the claimed structure. Since the multiplexer structure is disclosed in the examples, patent owner can at most argue that connecting different inputs to the multiplexer than the ones shown in the examples is a new use of an old machine. However, the use is not new since the multiplexers are intended to multiplex any set of inputs and, furthermore, the input signal variables are not part of the claimed structure. Also, a new use would have to be claimed as a process claim. 35 U.S.C. § 100(b).

(11)

Patent owner argues that the examiner errs in stating (at EA15-16) that input signals are all "input variables" regardless of whether or not they are set to a constant value because a constant (0 or 1) is not a variable (RBr16-17).

We agree that a constant (0 or 1) is not a variable. A variable must be capable of assuming, at any given time, either one of at least two values (0 or 1), whereas a constant has a fixed value. Gorai distinguishes between variables and constants; e.g., "the remaining 8 variables, or their complements or constant (0 or 1)" (page 164) and "[f]or the last stage g_p is

reduced to a single variable or constant 0 or 1" (page 166). However, since the input signals are not part of the claimed structure, it does not matter whether the inputs are variables or constant as long as the multiplexer is capable of handling variables.

It is argued (RBr17):

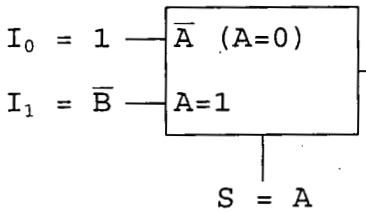
> When the input of a TG [transmission gate] is coupled to receive a variable, the TG functions as a multiplexer. When the input of a TG is coupled to receive a constant, the TG functions as a logic gate such as a NAND, NOR, or buffer. Representative logic gates coupled in this manner are shown in Exhibit D. If a constant were a variable, then the buffer circuit shown in Exhibit D would be a multiplexer. It is not.

This argument is incorrect. A multiplexer selects one of the input variables as an output and has the truth table shown in Table 1.4 (page 17) of Weste and in Exhibit D to the reply brief (where each "X" in Table 1.4 of West is a "don't care" that can be replaced by either a "0" or a "1" to give the truth table of Exhibit D). The multiplexer structure is the same whether the data inputs are variables or constants. The only difference is that there are fewer rows in the truth table when one or both inputs are a constant. Gorai discusses that the control inputs to a multiplexer are variables, while the data inputs can be a variable, its complement, or a constant (0 or 1) (page 165). As apparent from the example for an *M(3)* in Gorai (page 165), for a 2:1 multiplexer *M(1)*, there are two variables, two complements,

and a constant (0 or 1) (6 possible input values) that can be applied to each input , for a total of 6^2 distinct functions that can be realized. When the inputs are limited to variables, only 4^2 functions can be realized. In any case, the multiplexer performs as a multiplexer whether the inputs are constant, variables, or a mix of constants and variables.

The buffer in Exhibit D to the reply brief is a multiplexer with one input connected to the supply voltage V (a logical "1") and the other input connected to ground (a logical "0"). When the control variable A=1, the multiplexer selects the supply voltage V, and when A=0 ($\overline{A}$=1), the multiplexer selects ground. Similarly, the multiplexer for the NAND gate selects between a constant supply voltage V (a logical "1") and a variable complement $\overline{B}$. The multiplexer acts as a multiplexer regardless of whether the inputs are constants or variables. While patent owner has drawn the logic symbols, functions, and truth tables in Exhibit D to appear as different as possible from the those for the multiplexer, each logic function is, in fact, one connection

of the multiplexer. For example, a NAND gate can be drawn using the multiplexer symbol and function in Exhibit D:



$$
\begin{aligned}
f &= \overline{S}I_0 + SI_1 = \overline{A}\cdot 1 + A\cdot\overline{B} \\
&= \overline{A} + A\cdot\overline{B} \\
&= \overline{A} + \overline{B} \quad \text{(from: } a + \overline{a}b = a + b\text{)} \\
&= \overline{AB} \quad \text{(DeMorgan's law)}
\end{aligned}
$$

The multiplexer selects a "1" if A=0 and selects "$\overline{B}$" if A=1. The truth table with entries for all the inputs is

S=A	$I_1=\overline{B}$	$I_0=1$	F
0	0	1	1
0	1	1	1
1	0	1	0
1	1	1	1

This can be redrawn as a function of A and B as in Exhibit D. The truth table contains half the number of rows as the general multiplexer truth table because input I_0 is a constant.

(12)

Patent owner argues that the examiner errs in finding (at EA15) that the internal outputs of the first and second

multiplexer stages in Fig. 3 of Gorai are "input signals" (RBr17-18). It is argued that the examiner's interpretation of these internal signals as "input signals" is not reasonable because it strips the word "input" of meaning (RBr18).

The claims recite "input variables," not "input signals." We agree with patent owner that the outputs of the multiplexers can not be construed as the claimed "input variables." The claims recite that the TGM circuit signal input terminal not coupled to a previous stage output terminal is "coupled to receive" the "input variable"; thus, the TGM output cannot be an "input variable." However, the examiner points out that Fig. 3 of Gorai (for $p = 3$) shows seven input variables besides the two internal inputs from the multiplexers (EA15). Accordingly, it is not necessary to rely on the TGM outputs as "input variables" and the examiner's statement is harmless.

(13)

It is noted (RBr19) that the examiner's answer finds that "both Tosser and Gorai clearly teach 4:1 multiplexer circuits having three cascaded stages, and lack only the teaching to implement the stages using the well-known transmission gate multiplexer [TGM] circuits" (EA8). It is argued that "[i]f the Answer contends that, absent the recited TGM circuits, the rejections are based on some other modifications of either Tosser

or Gorai, or require features not found in either Tosser or Gorai, Patentee requests clarification and an opportunity to respond to such a rejection" (RBr19).

Patent owner correctly understands that the examiner finds the only difference between the claimed 4:1 multiplexer in claim 47 and the *p*-stage (with *p*=3) multiplexer in Gorai's Fig. 3 and the 3-stage multiplexer in Tosser is the use of TGMs. The examiner finds that the claimed 5:1 multiplexer with 4 stages in claim 48 is disclosed by the *p*-stage (with *p*=4) multiplexer in Gorai's Fig. 3 except for the TGMs. The examiner recognizes that a 4-stage serial multiplexer and the use of TGMs is not shown in Tosser, but concludes that one skilled in the art would have been motivated to modify the 3-stage multiplexer in Tosser to add an additional stage to allow processing of more input signals (FR7). This opinion does not alter the examiner's rejection.

(14)

Patent owner argues that the examiner incorrectly concluded that the licensing discussed in Mr. Tran's declaration under 37 C.F.R. § 1.132 concerning commercial success is mere potential licensing, whereas the declaration and accompanying exhibits demonstrate <u>actual</u>, not potential licensing (RBr19).

The only actual licensing is the licensing to Intel Corp. As discussed in the analysis of the objective evidence, it is not

known exactly what was licensed and patent owner has established no nexus between what was licensed and the claims of the '666 patent. The other evidence about discussions with Cadence, National Semiconductor, and Hewlett-Packard show only that these companies might be interested in something (not identified) by TTI, not that any licensing took place. We further agree with the examiner's appraisal that this evidence does not rise to the level of actual "licensing" or "commercial success" (EA23).

CONCLUSION

The rejections of claims 16, 17, 39-45, 47, and 48 are affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a). See 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

ERROL A. KRASS Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
ROBERT NAPPI Administrative Patent Judge	)	

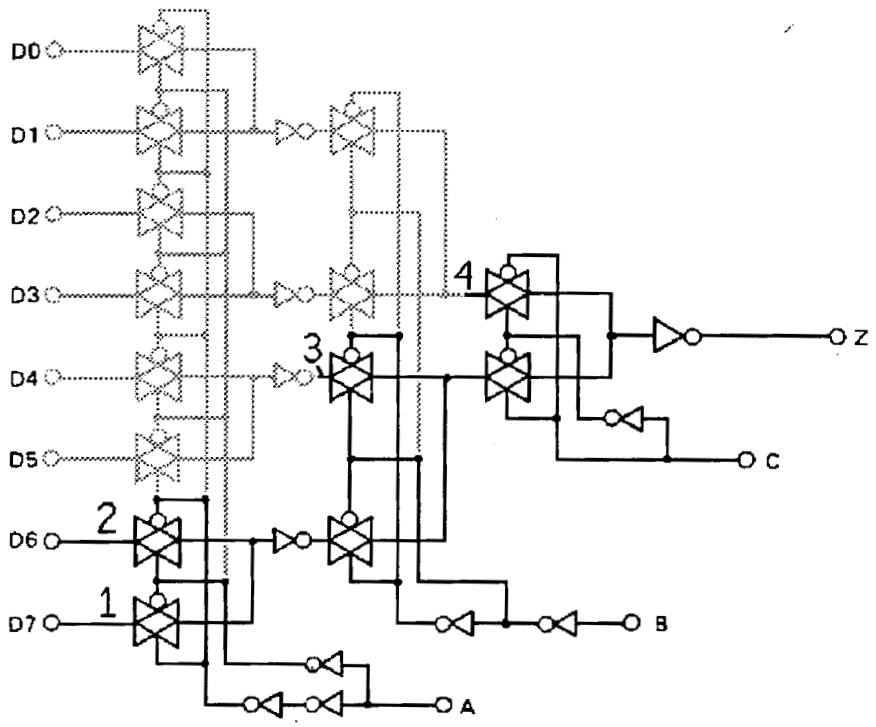
BARRETT, Administrative Patent Judge.

These additional comments are added because I think it should be pointed out that claim 47 is anticipated by the Toshiba TC19G000 Series, MUX8 Macrocell Data Sheet, page 1-110, May 1986, reproduced in Appendix D, and that claim 48 would have been obvious over Toshiba MUX8 in view of patent owner's admissions. I write separately because the panel does not want to raise any question of a new ground of rejection in the main opinion.

The Toshiba MUX8 reference was cited by the inventor in the background of the '666 patent (col. 1, lines 31-34). The Toshiba MUX8 multiplexer is a binary tree arrangement of 2:1 transmission gate multiplexers (TGMs) having four TGMs in the first stage controlled by control input A, two TGMs in the second stage controlled by control input B, and one TGM in the third stage controlled by control input C, forming an 8:1 multiplexer.

Claim 47 is an open-ended claim and does not preclude additional structure. It can be easily seen that the Toshiba MUX8 anticipates the subject matter of claim 47 from the figure on the next page in which the structure of claim 47 is shown in black lines (having four data input variables 1, 2, 3, and 4, and three control variables A, B, and C) and the additional structure not precluded by claim 47 is shown in gray.

SCHEMATIC



The instant reexaminations were all filed before the changes to 35 U.S.C. §§ 303(a) and 312(a) allowing consideration of old art in a reexamination proceeding. See In re Bass, 314 F.3d 575, 576 n.*, 65 USPQ2d 1156, 1157 n.* (Fed. Cir. 2002). Although we do not find any reference to the Toshiba MUX8 reference in the reexaminations, this may be because it was thought not to be permitted. This case is a good example of why old art, which may not have been fully appreciated by the examiner, should be allowed to be considered in a reexamination.

The '666 patent admits that known multiplexer circuits are built up of a binary tree arrangement of 2-input multiplexers and can have any number N input variables (col. 1, lines 9-39). In particular, there can be 16 multiplexer circuits in the first stage (col. 1, line 38), requiring four stages. It would have been obvious to one of ordinary skill in the art to extend the 8:1 binary tree arrangement of TGMs as taught by Toshiba MUX8 to a known 16:1 multiplexer in view of patentee's admission and such a four stage arrangement of 2:1 multiplexers contains the 5:1 multiplexer of claim 48.

Lee E. Barrett	)	BOARD OF PATENT
	)	APPEALS
LEE E. BARRETT	)	AND
Administrative Patent Judge	)	INTERFERENCES

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APPENDIX A

Gorai states that a conventional multiplexer with p control lines is designated as M(p) and "an M(p) can realize any function of (p+1) variables" (page 164). Patent owner argues that this means that a cascade of 2:1 multiplexers with p control input inputs can realize functions of <u>at most</u> (p+1) variables. This is incorrect because Gorai expressly discloses that "an M(p) having $p + k$ (= $p + 2^p$) inputs has the potential of realising functions of up to ($p + 2^p$) variables" (page 164); e.g., a 2:1 multiplexer (p=1, 2^p=2) can realize functions of up to three variables, one for the control input and two for the data inputs. However, for completeness, this appendix is provided to explain what is meant by "an M(p) can realize any function of (p+1) variables," using the example of an *M(1)* with 2 variables.

A function of two variables x_1, x_2 can be expressed as:

$$f(x_1, x_2) = A_3(x_1x_2) + A_2(x_1\overline{x_2}) + A_1(\overline{x_1}x_2) + A_0(\overline{x_1}\overline{x_2})$$

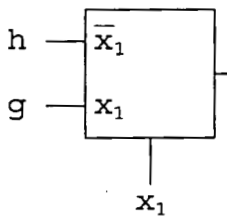
Where A_0, A_1, A_2, and A_3 are "0" or "1" as required to realize $f(x_1, x_2)$.[3] The statement "any function of [two] variables" means any function for any combination of A_0, A_1, A_2, and A_3 (i.e., a

---

[3] <u>See</u> C. Zhang, <u>Universal logic gate transmission gate array</u>, Electronic Engineering, October 1985 (of record), page 63, middle and right columns (note that the expression $f(x_1,x_2) = x_2p + x_2q$ should obviously be $f(x_1,x_2) = \overline{x_2}p + x_2q$).

function composed of zero terms, any one term, any two terms, any three terms, or all four terms). There can be several ways to connect the inputs of an *M(1)* to implement a function, but we assume the control input is x_1 and the data inputs can be 0, 1, x_2, $\overline{x_2}$. There are 16 logic functions of 2 variables.

An *M(1)* for a function of two variables x_1, x_2 is shown below (Gorai, Fig. 2a, page 165):



$$f = gx_1 + h\overline{x}_1$$

where h, g can assume any value 0, 1, x_2, or $\overline{x}_2$

The functions of zero, one, two, three, and four terms are listed below. The distributive law, $A\cdot(B+C)=(A\cdot B)+(A\cdot C)$, the relationship, $A+\overline{A}=1$, the relationship, $A+\overline{A}B=A+B$, and DeMorgan's laws, $\overline{A}+\overline{B}=\overline{AB}$ and $\overline{A+B}=\overline{A}\,\overline{B}$, are used to simplify the expressions.

<u>0 terms at a time:</u>

$$f(x_1,x_2) = 0 \qquad = 0$$

<u>1 term at a time:</u>

$$\begin{aligned}
f(x_1,x_2) &= \overline{x_1}\,\overline{x_2} &&= \overline{x_1}\,\overline{x_2}\\
&&&= \overline{x_1+x_2}\\
f(x_1,x_2) &= \overline{x_1}x_2 &&= \overline{x_1}x_2\\
f(x_1,x_2) &= x_1\overline{x_2} &&= x_1\overline{x_2}\\
f(x_1,x_2) &= x_1x_2 &&= x_1x_2
\end{aligned}$$

<u>2 terms at a time:</u>

$$\begin{aligned}
f(x_1,x_2) &= x_1x_2 + x_1\overline{x_2} &&= x_1(x_2+\overline{x_2})\\
&&&= x_1\\
f(x_1,x_2) &= x_1x_2 + \overline{x_1}x_2 &&= (x_1+\overline{x_1})x_2\\
&&&= x_2\\
f(x_1,x_2) &= x_1x_2 + \overline{x_1}\,\overline{x_2} &&= x_1x_2 + \overline{x_1}\,\overline{x_2}\\
f(x_1,x_2) &= x_1\overline{x_2} + \overline{x_1}x_2 &&= x_1\overline{x_2} + \overline{x_1}x_2\\
f(x_1,x_2) &= x_1\overline{x_2} + \overline{x_1}\,\overline{x_2} &&= (x_1+\overline{x_1})\overline{x_2}\\
&&&= \overline{x_2}\\
f(x_1,x_2) &= \overline{x_1}x_2 + \overline{x_1}\,\overline{x_2} &&= \overline{x_1}(x_2+\overline{x_2})\\
&&&= \overline{x_1}
\end{aligned}$$

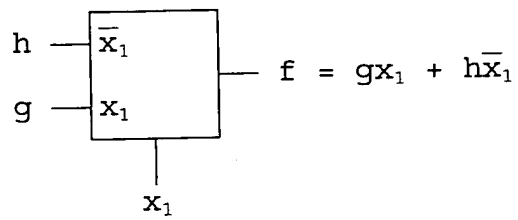
<u>3 terms at a time:</u>

$$\begin{aligned}
f(x_1,x_2) &= x_1x_2 + x_1\overline{x_2} + \overline{x_1}x_2 &&= x_1 + \overline{x_1}x_2\\
&&&= x_1 + x_2\\
f(x_1,x_2) &= x_1x_2 + x_1\overline{x_2} + \overline{x_1}\,\overline{x_2} &&= x_1 + \overline{x_1}\,\overline{x_2}\\
&&&= x_1 + \overline{x_2}\\
f(x_1,x_2) &= x_1x_2 + \overline{x_1}x_2 + \overline{x_1}\,\overline{x_2} &&= \overline{x_1} + x_1x_2\\
&&&= \overline{x_1} + x_2\\
f(x_1,x_2) &= x_1\overline{x_2} + \overline{x_1}x_2 + \overline{x_1}\,\overline{x_2} &&= \overline{x_1} + x_1\overline{x_2}\\
&&&= \overline{x_1} + \overline{x_2}\\
&&&= \overline{x_1x_2}
\end{aligned}$$

<u>All 4 terms:</u>

$$\begin{aligned}
f(x_1,x_2) &= x_1x_2 + x_1\overline{x_2} + \overline{x_1}x_2 + \overline{x_1}\,\overline{x_2} &&= x_1(x_2+\overline{x_2}) + \overline{x_1}(x_2+\overline{x_2})\\
&&&= x_1 + \overline{x_1}\\
&&&= 1
\end{aligned}$$

These functions of $f(x_1, x_2)$ can be summarized below.



$A_3 A_2 A_1 A_0$	Canonical form	$f(x_1, x_2) =$	Function	h	g
0 0 0 0	0	0	0	0	0
0 0 0 1	$\bar{x}_1\bar{x}_2$	$\overline{x_1+x_2}$	NOR (x_1, x_2)	$\bar{x}_2$	0
0 0 1 0	$\bar{x}_1 x_2$	$\bar{x}_1 x_2$		x_2	0
0 0 1 1	$\bar{x}_1 x_2 + \bar{x}_1\bar{x}_2$	$\bar{x}_1$	NOT (x_1)	1	0
0 1 0 0	$x_1\bar{x}_2$	$x_1\bar{x}_2$		0	$\bar{x}_2$
0 1 0 1	$x_1\bar{x}_2 + \bar{x}_1\bar{x}_2$	$\bar{x}_2$	NOT (x_2)	$\bar{x}_2$	$\bar{x}_2$
0 1 1 0	$x_1\bar{x}_2 + \bar{x}_1 x_2$	$x_1\bar{x}_2 + \bar{x}_1 x_2$	XOR (x_1, x_2)	x_2	$\bar{x}_2$
0 1 1 1	$x_1\bar{x}_2 + \bar{x}_1 x_2 + \bar{x}_1\bar{x}_2$	$\overline{x_1 x_2}$	NAND (x_1, x_2)	1	$\bar{x}_2$
1 0 0 0	$x_1 x_2$	$x_1 x_2$	AND (x_1, x_2)	0	x_2
1 0 0 1	$x_1 x_2 + \bar{x}_1\bar{x}_2$	$x_1 x_2 + \bar{x}_1\bar{x}_2$	XNOR (x_1, x_2)	$\bar{x}_2$	x_2
1 0 1 0	$x_1 x_2 + \bar{x}_1 x_2$	x_2	BUFFER (x_2)	x_2	x_2
1 0 1 1	$x_1 x_2 + \bar{x}_1 x_2 + \bar{x}_1\bar{x}_2$	$\bar{x}_1 + x_2$		1	x_2
1 1 0 0	$x_1 x_2 + x_1\bar{x}_2$	x_1	BUFFER (x_1)	0	1
1 1 0 1	$x_1 x_2 + x_1\bar{x}_2 + \bar{x}_1\bar{x}_2$	$x_1 + \bar{x}_2$		$\bar{x}_2$	1
1 1 1 0	$x_1 x_2 + x_1\bar{x}_2 + \bar{x}_1 x_2$	$x_1 + x_2$	OR (x_1, x_2)	x_2	1
1 1 1 1	$x_1 x_2 + x_1\bar{x}_2 + \bar{x}_1 x_2 + \bar{x}_1\bar{x}_2$	1	1	1	1

Therefore, an *M(1)* can realize all possible functions of two variables. Note that (h, g) include all combinations of the four possible inputs $(0, 1, x_2, \bar{x}_2)$. Note also that the truth table for each function is given by the coefficients $A_3 A_2 A_1 A_0$:

x_1	x_2	f
0	0	A_0
0	1	A_1
1	0	A_2
1	1	A_3

While a 2:1 multiplexer can realize functions of three variables, one control variable and two data input variables, it can <u>not</u> realize <u>all</u> functions of three variables. Because of the multiplexer structure, which selects one of the two inputs according to the control variable, an output term can have only two variables, a control variable and one of the input variables, and cannot have all three variables. Conventional multiplexers having p control inputs and k data inputs can implement all functions of $(p+1)$ variables because the p control variables select one of the k input variables.

APPENDIX B

Although the terminology and expressions in Gorai and Tosser are self-evident to any computer scientist or electrical engineer who has taken an undergraduate computer science course in switching theory and the design of digital logic circuits, we provide some explanation for readers of this opinion who lack this technical background.

TERM	DEFINITION
"variable"	A symbol that may take on either of the logical values "0" or "1." In positive logic, variable x is "1" when x=1, and its complement $\bar{x}$ is "1" when x=0.
"literal"	Variable or its complement (x, $\bar{x}$, etc.)
"product term"	Series of literals related by AND, written as a product, e.g., $x_1 \cdot x_2$ or $x_1 x_2$ (x_1 AND x_2). A product term is a term for which the function is equal to a logical "1." A product term is equal to a logical "1" if each variable and variable complement is equal to a logical "1"; otherwise it is "0." For example, for x_1=1, x_2=0, x_3=0, $x_1\bar{x}_2\bar{x}_3 = 1 \cdot 1 \cdot 1 = 1$, and $x_1\bar{x}_2x_3 = 1 \cdot 1 \cdot 0 = 0$.
"sum term"	Series of literals related by OR, written with "+" sign, e.g., $x_1 + x_2$ (x_1 OR x_2).
"minterm"	A "product term" that contains as many literals as there are variables in the function, e.g., if a function involves variables x_1, x_2, and x_3, then $\bar{x}_1\bar{x}_2\bar{x}_3$, $\bar{x}_1\bar{x}_2x_3$, $\bar{x}_1x_2\bar{x}_3$, $\bar{x}_1x_2x_3$, $x_1\bar{x}_2\bar{x}_3$, $x_1\bar{x}_2x_3$, $x_1x_2\bar{x}_3$, and $x_1x_2x_3$ are the eight possible minterms. A minterm, being a product term, is equal to a logical "1" if each variable and complement is "1."

"minterm table"

A table whose rows are minterms, i.e., for which the function has the value "1." The rows may be numbered as the decimal equivalents on the input combinations on each row interpreted as binary numbers. One example is the function of four variables (page 167):

$$f_2(x_1,x_2,x_3,x_4) = \Sigma(0,5,7,8,9,12,13)$$

The "Σ" sign means that the terms in the parenthesis are all connected by "+" (OR). That is, $f_2=1$ when $(x_1,x_2,x_3,x_4)=0$ OR 5 OR 7 OR 8 OR 9 OR 12 OR 13. Each term is just the decimal equivalent of the binary number, e.g., $f_2(x_1,x_2,x_3,x_4)=5$ corresponds to the row $x_1=0$, $x_2=1$, $x_3=0$, and $x_4=1$ (5 in binary) in the minterm table.

"sum of products"

A sum of product terms, e.g., $x_1\bar{x}_2\bar{x}_3 + \bar{x}_1\bar{x}_2x_3$.

"standard sum of products" or "canonical form"

Sum of products terms where every product term is a minterm, e.g., if a function involves variables x_1, x_2, and x_3, then $x_1\bar{x}_2\bar{x}_3 + \bar{x}_1\bar{x}_2x_3$ is one possible standard sum of products. Any switching function of n variables $f(x_1, x_2, \ldots, x_n)$ may be expressed as a standard sum of products.

"switching function"

In logic circuits, a fixed number of variables, say *n*, serve as inputs to a circuit under consideration. There are 2^n possible ways of assigning values to *n* variables. The two-variable case is illustrated in the truth table below.

x	y	F
0	0	?
0	1	?
1	0	?
1	1	?

If the four question marks are replaced by any combination of zeros and ones, a specific *function* of x_1 and x_2 is defined. There are $2^4 = 16$ ways of replacing the four question marks by zeros and ones, so there are 16 *switching functions* of two variables. A "switching function" of *n* variables is any one particular assignment of functional

values (1s or 0s) for all 2^n possible combinations of values of the *n* variables. There are many *expressions* for a given switching function. For example, it can be determined that

$$x + xy + y + yz$$
$$x + \bar{x}y + x(w + \bar{w})$$
$$x + y$$

are all expressions for the same function, specifically the logical OR function in the following truth table.

x	y	F
0	0	0
0	1	1
1	0	1
1	1	1

APPENDIX C

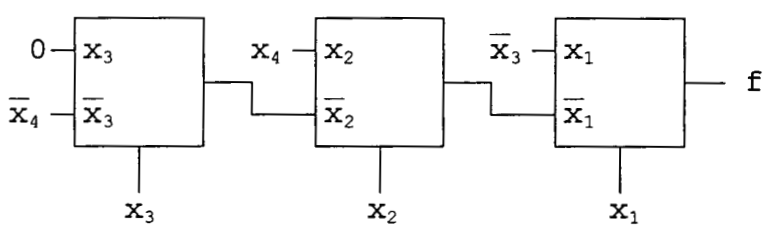
The rejection does not need to rely on the examples in Gorai. Nevertheless, in view of patent owner's arguments that the combinational logic circuits in Gorai and Tosser are not multiplexers, it may be useful to show how the examples use multiplexers to realize functions.

(1)

Consider the function of Example 2 (page 167):

$$f_2(x_1,x_2,x_3,x_4) = \Sigma(0,5,7,8,9,12,13)$$

This function is realized by the circuit of Gorai's Fig. 6, which we have redrawn below to show the correspondence between the input variables and the control variables.



There are four paths through the multiplexer and anyone with minimal background in logical circuits using Gorai can see that the resulting function is, starting from the right:

$$f_2(x_1,x_2,x_3,x_4) = x_1\bar{x}_3 + \bar{x}_1(x_2x_4 + \bar{x}_2(x_3 \cdot 0 + \bar{x}_3\bar{x}_4))$$
$$= x_1\bar{x}_3 + \bar{x}_1x_2x_4 + \bar{x}_1\bar{x}_2\bar{x}_3\bar{x}_4$$

Where a term does not include all variables, these missing variables are "don't cares" and can be replaced by "0" and "1." The terms can be expanded using the identity $A+\overline{A}=1$ to get the function in the form of minterms:

$$
\begin{aligned}
f_2 &= x_1(x_2+\overline{x}_2)\overline{x}_3(x_4+\overline{x}_4) + \overline{x}_1x_2(x_3+\overline{x}_3)x_4 + \overline{x}_1\overline{x}_2\overline{x}_3\overline{x}_4 \\
&= x_1\overline{x}_2\overline{x}_3\overline{x}_4 + x_1\overline{x}_2\overline{x}_3x_4 + x_1x_2\overline{x}_3\overline{x}_4 + x_1x_2\overline{x}_3x_4 \\
&\quad + \overline{x}_1x_2\overline{x}_3x_4 + \overline{x}_1x_2x_3x_4 + \overline{x}_1\overline{x}_2\overline{x}_3\overline{x}_4
\end{aligned}
$$

It can be easily seen that

$$
\begin{aligned}
\overline{x}_1\overline{x}_2\overline{x}_3\overline{x}_4 &= 0000 = 0 \\
\overline{x}_1x_2\overline{x}_3x_4 &= 0101 = 5 \\
\overline{x}_1x_2x_3x_4 &= 0111 = 7 \\
x_1\overline{x}_2\overline{x}_3\overline{x}_4 &= 1000 = 8 \\
x_1\overline{x}_2\overline{x}_3x_4 &= 1001 = 9 \\
x_1x_2\overline{x}_3\overline{x}_4 &= 1100 = 12 \\
x_1x_2\overline{x}_3x_4 &= 1101 = 13
\end{aligned}
$$

These are the minterms for which the function equals 1. This is one example of how a multiplexer implements a function.

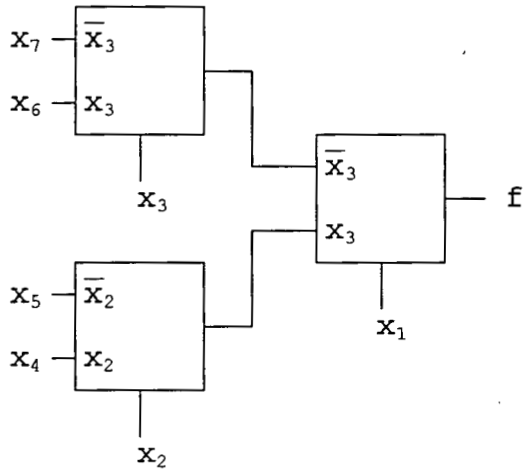
(2)

Gorai considers the function (page 165):

$$f = x_1x_2x_4 + x_1\overline{x}_2x_5 + \overline{x}_1x_3x_6 + \overline{x}_1\overline{x}_3x_7$$

Gorai states that "[t]his function can be realised by a network of three 2-input multiplexers" (*Id.*) While this indicates that three 2-input multiplexers can implement a function of seven

variables, it is noted that the implementation is not a series arrangement of multiplexers, but looks like this:



APPENDIX D

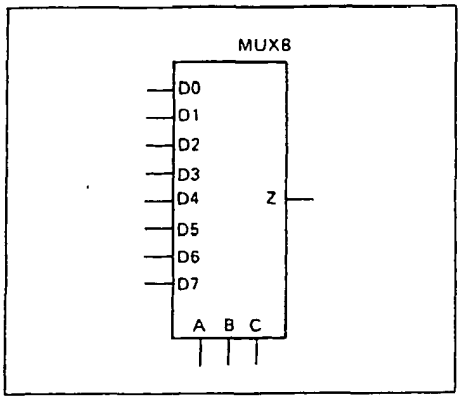
TC19G000 SERIES

MACROCELL DATA SHEET

MUX8 MUX8

CELL NAME	FUNCTION	CELL COUNT	
MUX8	8 TO 1 MULTIPLEXER	BASIC	13
		I/O	0

LOGIC SYMBOL



TRUTH TABLE

SELECT INPUT			OUTPUT
C	B	A	Z
L	L	L	D0
L	L	H	D1
L	H	L	D2
L	H	H	D3
H	L	L	D4
H	L	H	D5
H	H	L	D6
H	H	H	D7

AC CHARACTERISTICS

	TpLH		TpHL	
	Tup	Kup	Tdn	Kdn
Dn → Z	2.05	0.11	2.32	0.15
A → Z	3.45	0.11	3.72	0.15
B → Z	2.75	0.11	3.02	0.15
C → Z	1.60	0.11	1.38	0.15
UNIT	nS	nS/LU	nS	nS/LU

TDL DESCRIPTION

```
Name (Z) = MUX8 (D0, D1, D2, D3, D4, D5,
                 D6, D7, A, B, C);
```

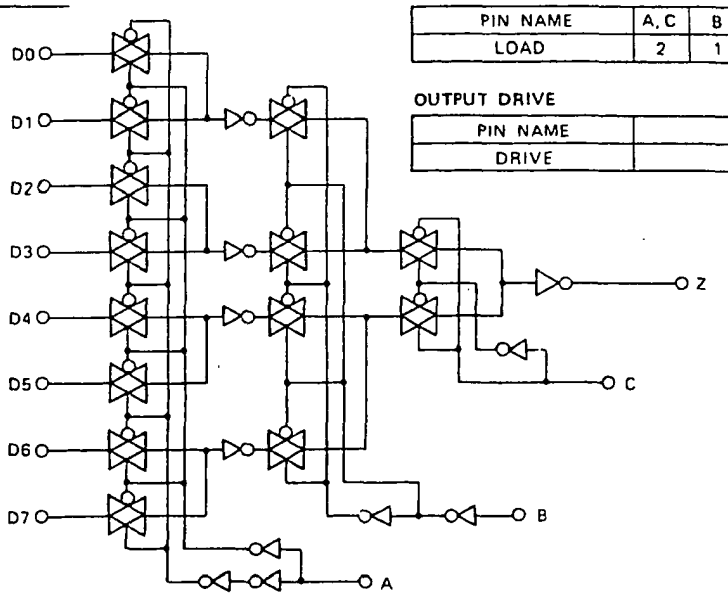
INPUT LOAD (LU)

PIN NAME	A, C	B	D0 ~ D7
LOAD	2	1	2.69

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	27.0

SCHEMATIC



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