

The opinion in support of the decision being entered today was *not* written for publication and is *not* binding precedent of the Board.

**UNITED STATES PATENT AND TRADEMARK OFFICE**

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**BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES**

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*Ex parte* AHMAD R. ANSARI

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Appeal No. 2005-2273  
Application No. 10/319,026

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ON BRIEF

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Before HAIRSTON, BARRY, and LEVY, *Administrative Patent Judges*.  
BARRY, *Administrative Patent Judge*.

A patent examiner rejected claims 21-26.<sup>1</sup> The appellant appeals therefrom under 35 U.S.C. § 134(a). We reverse and enter a new ground of rejection.

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<sup>1</sup>More specifically, claims 21-26 include independent claim 21 and dependent claims 22, 23, 24, 25a, 25b, and 26. "If there are several claims, they shall be numbered consecutively in Arabic numerals." 37 C.F.R. § 1.75(f). Here, the rejected claims include claims labeled "25a" and "25b." (Amended Appeal Br. at 2.) Being "basically a board of review," *Ex parte Gambogi*, 62 USPQ2d 1209, 1211 (Bd.Pat.App. & Int. 2001), we leave the question of whether such alphanumeric labeling satisfies the aforementioned requirement for consecutive numbering in numerals to the examiner and the appellant.

## I. BACKGROUND

The invention at issue on appeal concerns computer memory for handling vector data. (Spec. at 1.) Multimedia applications "present a very high level of parallelism by performing vector-like operations on large data sets." (*Id.* at 3.) Although architectural extensions have addressed the computational demands of multimedia programs, opines the appellant, "the memory bandwidth requirements of these applications have generally been ignored." (*Id.*) He adds, "Data caches in current general-purpose processors are not large enough to hold these vector data sets which tend to pollute the caches very quickly with unnecessary data and consequently degrade the performance of other applications running on the processor." (*Id.*)

Accordingly, the appellant's invention is a vector transfer unit ("VTU") for transferring sets of vector data into and out of a processor. Such transfers bypass any data cache used by the processor. (*Id.* at 4.)

A further understanding of the invention can be achieved by reading the following claim:

21. A circuit comprising a microprocessor, the microprocessor comprising:
  - a register file comprising a plurality of registers for storing vector data;

a vector transfer unit coupled to the register tile, wherein the vector transfer unit comprises a dual port memory for storing vector data and a vector transfer execution unit coupled to the dual port memory, wherein the vector transfer execution unit comprises a vector transfer instruction queue for storing load/store and move vector data instructions;

wherein the vector transfer execution unit transfers vector data between a main memory and the dual port memory in response to the vector transfer execution unit executing a load/store vector data instruction stored in the vector transfer instruction queue;

wherein the vector transfer execution unit transfers vector data between the dual port memory and one or more registers of the register file in response to the vector transfer execution unit executing a move vector data instruction stored in the vector transfer instruction queue.

Claims 21, 22, and 26 stand rejected under 35 U.S.C. § 103(a) as obvious over U.S. Patent No. 5,689,653 ("Karp") and U.S. Patent No. 5,487,156 ("Popescu"), with a definition of the term "cache" from the *Free On-Line Dictionary of Computing* ("FOLDOC") cited as extrinsic evidence. Claims 23, 24, 25a, and 25b stand rejected under § 103(a) as obvious over Karp; Popescu; and U.S. Patent No. 4,594,682 ("Drimak"), with FOLDOC cited as extrinsic evidence.

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## II. OPINION

Our opinion addresses the rejections in the following order:

- Examiner's rejections
- Board's rejection.

### A. EXAMINER'S REJECTIONS

"Rather than reiterate the positions of the examiner or the appellant *in toto*, we focus on the point of contention therebetween." *Ex parte Kaysen*, No. 2003-0553, 2004 WL 1697755, at \*2 (Bd.Pat.App & Int. 2004). The examiner admits, "Karp et al. did not teach that the vector transfer execution unit comprised a vector transfer instruction queue for storing the instructions." (Examiner's Answer at 5.) Finding that "Popescu et al. taught an instruction queue for storing instructions awaiting execution (fig. 2, 11)," (*id.*), he offers the following assertion.

[T]emporary imbalances between the rate that instructions are issued and executed arise because Karp et al. implements a cache memory (see col. 3 lines 28-29, col. 4 lines 5-9, and claim 1, lines 2-3). As is shown by the extrinsic evidence of the FOLDOC definition of cache, a cache is accessed more quickly than main memory: "The cache is built from faster memory chips than main memory so a cache hit takes much less time to complete than a normal memory access." As it is impossible to issue an instruction before it is fetched from memory, the fact that fetching of instructions will have temporary rate imbalances (because a hit in cache

will be satisfied much more quickly than a miss in cache, see FOLDOC definition) results in the issue rate also having temporary rate imbalances.

(*Id.* at 10.) Based on this assertion, the examiner concludes, "addition of a queue as taught by Popescu to smooth those temporary rate imbalances would have been obvious to one of ordinary skill in the art at the time of invention." (*Id.*) The appellant argues, "An imbalance between the rate instructions are issued and the rate issued instructions are executed depends on the speed at which instructions are executed. If Karp employs a processor that executes instructions faster than instructions are issued, there will be no adverse rate imbalance regardless of whether the instructions issue from a cache memory or from normal memory." (Reply Br. at 3)

"In addressing the point of contention, the Board conducts a two-step analysis. First, we construe the independent claim at issue to determine its scope. Second, we determine whether the construed claim would have been obvious." *Ex parte Sehr*, No. 2003-2165, 2005 WL 191041, at \*3 (Bd.Pat.App & Int. 2004).

### 1. Claim Construction

"Analysis begins with a key legal question — *what is the invention claimed?*" *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561, 1567, 1 USPQ2d 1593, 1597 (Fed. Cir. 1987). In answering the question, "the Board must give claims their broadest reasonable construction. . . ." *In re Hyatt*, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1668 (Fed. Cir. 2000). "Moreover, limitations are not to be read into the claims from the specification." *In re Van Geuns*, 988 F.2d 1181, 1184, 26 USPQ2d 1057, 1059 (Fed. Cir. 1993) (citing *In re Zletz*, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989)).

Here, claim 21<sup>2</sup> recites in pertinent part the following limitations: "a vector transfer instruction queue for storing load/store and move vector data instructions." Giving the independent claim its broadest, reasonable construction, the limitations require a queue for storing vector instructions.

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<sup>2</sup>The appellant's Amended Appeal Brief (p. 2) inadvertently refers to the sole independent claim on appeal as "independent claim 26."

## 2. Obviousness Determination

"Having determined what subject matter is being claimed, the next inquiry is whether the subject matter would have been obvious." *Ex Parte Massingill*, No. 2003-0506, 2004 WL 1646421, at \*3 (Bd.Pat.App & Int. May 20, 2004). "In rejecting claims under 35 U.S.C. Section 103, the examiner bears the initial burden of presenting a *prima facie* case of obviousness." *In re Rijckaert*, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993) (citing *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992)). A *prima facie* case of obviousness is "based on underlying factual determinations including . . . what th[e] prior art teaches explicitly and inherently. . . ." *In re Zurko*, 258 F.3d 1379, 1383, 59 USPQ2d 1693, 1696 (Fed. Cir. 2001) (citing *Graham v. John Deere Co.*, 383 U.S. 1, 17-18, 148 USPQ 459, 467 (1966); *In re Dembiczak*, 175 F.3d 994, 998, 50 USPQ 1614, 1616 (Fed. Cir. 1999); *In re Napier*, 55 F.3d 610, 613, 34 USPQ2d 1782, 1784 (Fed. Cir. 1995)).

Here, the examiner admits, "Karp et al. did not explicitly state that temporary imbalances between the rate that instructions are issued and executed arise in his system." (Examiner's Answer at 6.) Instead, the examiner relies on his aforementioned assertion that such temporary imbalances are inherent to Karp. "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that

it would be so recognized by persons of ordinary skill." *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999) (quoting *Continental Can Co. v. Monsanto Co.*, 948 F.2d 1264, 1268, 20 USPQ2d 1746, 1749 (Fed. Cir. 1991))

"Inherency . . . may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." *In re Oelrich*, 666 F.2d 578, 581, 212 USPQ 323, 326 (CCPA 1981) (citing *Hansgirg v. Kemmer*, 102 F.2d 212, 214, 40 USPQ 665, 667 (Cust. & Pat.App. 1939)).

Here, Karp "relates to a computer system utilizing vector memory operations to exchange data with memory." Col. 1, ll. 6-7. More specifically, the "computer system 20 . . . comprises a processor 22 which is connected to a memory 24 and peripheral devices 26 with a multiple signal system bus 30. The processor 22 preferably includes a high speed cache memory." Col. 3, ll. 23-29. For its part, "[t]he memory 24 . . . is made up of various types of memory, including a primary or main memory. . . . The memory 24 stores data and instructions for one or more programs that implement a desired task or calculation on the computer system 20." *Id.* at ll. 29-37. The reference collectively characterizes the aforementioned memories as a "memory hierarchy 46." *Id.* at l. 66.

Karp further explains that an "instruction issue unit 56 decodes instructions of a currently executing program read by the processor 22 (FIG. 1) from the memory 24 (FIG. 1) and issues control signals directing execution of corresponding operations within the processor. Vector data transfers between the memory hierarchy 46 and . . . vector buffers 50-52 are initiated by the instruction issue unit 56 in response to vector request instructions in the currently executing program. These vector request instructions specify information identifying the vector in the memory hierarchy 46 which is to be the subject of a vector data transfer." Col. 4, ll. 46-56.

Turning to FOLDOC, it is uncontested that "a cache hit takes much less time to complete than a normal memory access." P. 1. Nonetheless, we are unpersuaded that "temporary imbalances between the rate that instructions are issued and executed," (Examiner's Answer at 10), **necessarily** arise in Karp and would be so recognized by persons of ordinary skill in the art. To the contrary, we agree with the appellant that "[i]f Karp employs a processor that executes instructions faster than instructions are issued, there will be no adverse rate imbalance regardless of whether the instructions issue from a cache memory or from normal memory." (Reply Br. at 3) In other words, the reference's processor 22 may execute its vector instructions fast enough to preclude any rate imbalance regardless of whether the instructions are fetched from its

high speed cache memory or from its memory 24. The mere fact that temporary imbalances between the rate that instructions are issued and executed may arise in Karp is insufficient as a motivation to combine teachings of Karp and Popescu.

The examiner does not allege, let alone show, that the addition of Drimak cures the aforementioned deficiency of Karp, Popescu, and FOLDOC. Absent a teaching or suggestion of a queue for storing vector instructions, we are unpersuaded of a *prima facie* case of obviousness. Therefore, we reverse the obviousness rejection of claim 21 and of claims 22-26, which depend therefrom.

#### B. BOARD'S REJECTION

Under 37 C.F.R. § 41.50(b)(2005), we enter a new ground of rejection against claim 21. "A *prima facie* case of obviousness is established when the teachings from the prior art itself would appear to have suggested the claimed subject matter to a person of ordinary skill in the art." *In re Bell*, 991 F.2d 781, 783, 26 USPQ2d 1529, 1531 (Fed. Cir. 1993) (quoting *In re Rinehart*, 531 F.2d 1048, 1051, 189 USPQ 143, 147 (CCPA 1976)).

Here, we reject claim 21 under § 103(a) as obvious over Karp and Murray Sargent III and Richard Shoemaker ("Sargent"), *The IBM Personal Computer™ from the*

*Inside Out* (rev. ed. 1986). As found by the examiner, (Examiner's Answer at 5), Karp teaches the following limitations of claim 21:

A circuit	fig. 1
comprising a microprocessor, the microprocessor comprising:	22
a register file comprising a plurality of registers for storing vector data	fig. 2, 58, 42, 43, col. 2 lines 52-57
a vector transfer unit	60-62, 50-52, 64-66
[c]oupled to the register file	58, 42, 43
wherein the vector transfer unit comprises a dual port memory for storing vector data and	50, 51, 52, each buffer showing an both an incoming and outgoing port, two ports equaling "dual port"
a vector transfer execution unit coupled to the dual port memory	70, 71, 72
wherein the vector transfer execution unit operates upon load/store and move vector data instructions	col. 4 lines 50-60, the disclosed "vector request instructions" covers load, store, and move.
wherein the vector transfer execution unit	70, 71, 72
transfers vector data between a main memory and	46, col. 6 line 48 to col. 8 line 7
the dual port memory	50, 51, 52
in response to the vector transfer execution unit	70, 71, 72
executing a load/store vector data instruction	col. 4 lines 50-60
wherein the vector transfer execution unit transfer[s] vector data between the dual port memory	70, 71, 72 50, 51, 52
and one or more registers of the register file	58, 42, 43
in response to the vector transfer execution unit executing a move vector data instruction	col. 4 lines 50-60

Furthermore, we find that the reference seeks to increase "[t]he speed at which data can be transferred between a computer system's processor and memory [,which] is sometimes referred to as its memory bandwidth." Col. 1, ll. 33-35.

We also find that Sargent discloses the inclusion of an "instruction-fetch queue" in a processor. P. 218 (copy attached). "Its purpose is to speed up program execution." *Id.* Because Karp seeks to speed operations, and Sargent teaches a queue to speed operations, we find that a person having ordinary skill in the art to which the subject matter pertains would have been motivated to employ a queue for storing vector instructions to speed up program execution. We conclude that such a combination of teachings would have made claim 21 obvious to a person having ordinary skill in the art to which the subject matter pertains.

In an *ex parte* appeal, "the Board is basically a board of review — we review . . . rejections made by patent examiners." *Gambogi*, 62 USPQ2d at 1211. Accordingly, we leave any further determination of the obviousness of claims 22-26 in view of Karp and Sargent to the examiner and the appellant.

### III. CONCLUSION

In summary, the examiner's rejections of claims 21-26 under § 103(a) are reversed. A new rejection of claim 21 under § 103(a), however, is added.

37 C.F.R. § 41.50(b) provides that "[a] new grounds of rejection pursuant to this paragraph shall not be considered final for judicial review." Section 41.50(b) also provides that, within two months from the date of the decision, the appellant must exercise one of the following options to avoid termination of proceedings of the rejected claims:

- (1) Submit an appropriate amendment of the claims so rejected or new evidence relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the proceeding will be remanded to the examiner. . . .
- (2) Request that the proceeding be reheard under 37 C.F.R. § 41.52 by the Board upon the same record. . . .

No time for taking any action connected with this appeal may be extended under 37 C.F.R. § 1.136(a).

REVERSED  
37 C.F.R. § 41.50(b)

KENNETH W. HAIRSTON  
Administrative Patent Judge

LANCE LEONARD BARRY  
Administrative Patent Judge

STUART S. LEVY  
Administrative Patent Judge

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Appeal No. 2005-2273  
Application No. 10/319,026

Page 15

CAMPBELL STEPHENSON ASCOLESE, LLP  
4807 SPICEWOOD SPRINGS RD.  
BLDG. 4, SUITE 201  
AUSTIN, TX 78759