The opinion in support of the decision being entered today was *not* written for publication and is *not* binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte Robert W. St. John and Joseph L. Temple III

Appeal No. 2005-2279
Application No. 09/515,432

ON BRIEF

Before HAIRSTON, JERRY SMITH, and BARRY, *Administrative Patent Judges*.
BARRY, *Administrative Patent Judge*.

A patent examiner rejected claims 1-6, 9-11, 13-18, 21-30, 33, and 34. The appellants appeal therefrom under 35 U.S.C. § 134(a). We reverse and enter a new ground of rejection.

I. BACKGROUND

The invention at issue on appeal concerns prefetching instructions for a computer processor executing a computer program. "Modern computer architectures typically cache instructions in a dedicated instruction cache and have various mechanisms for loading the cache efficiently." (Spec. at 1.) Such mechanisms involve prefetching instructions in the next sequential block from where a processor is currently

executing. "Branching interrupts this flow and history tables are conventionally used to determine the most likely branch to prefetch along." (*Id.*) These techniques work well for classically written, procedural programs, which tend to have reasonable working sets and iterate "inner loops" of densely packed code explain the appellants. (*Id.*)

The appellants further explain that non-procedural programs, such as object-oriented code, include "many more unconditional branch and link operations[,] which may or may not be iterated." (*Id.*) Consequently, they opine, "object-oriented code typically suffers from degraded cache hit ratios and the classical next sequential block prefetch is often ineffective and may result in degradation of performance of the [associated computer] system." (*Id.* at 1-2.)

In contrast, the appellants' invention works to predict a "call path," which the appellants assert, improves prefetching "even when there is little locality of reference either from sequential execution or 'tight loops'." (*Id.* at 4.) More specifically, the appellants compile an update prefetch stream ("UPS") instruction into a non-procedural program, such as object-oriented code. The UPS instruction is preferably compiled several instructions before an unconditional branch and link ("BAL") instruction, for example, where code of a first object calls code of a second object. The UPS instruction causes loading of an x,y address pair into a prefetch buffer. When an

incremented prefetch address matches an x address of the x,y address pairs loaded into the prefetch buffer, the corresponding new memory address y is substituted for the incremented prefetch address, thereby effecting the jump in memory address prefetching. (*Id.* at 3.)

A further understanding of the invention can be achieved by reading the following claim.

> 1. A method for implementing prefetching of instructions for a processor executing a non-procedural program, said method comprising:
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> prefetching instructions into a cache from memory which are sequential instructions from where the processor is currently executing in a sequence of instructions of said non-procedural program; and
>
> wherein when said prefetching encounters an update prefetch stream instruction, said prefetching comprises executing said update prefetch stream instruction to load at least one address pair into a set associative array of x,y address pairs, wherein the at least one address pair is independent of a specific currently pending branch instruction, and subsequent thereto, changing a current prefetch address to a new memory prefetch address for prefetching of at least one non-sequential instruction from memory for loading into the cache, said changing comprising comparing a current prefetch address with each x address of the set of associative array of x,y address pairs, and if a match is found, changing to a new memory prefetch address y paired with the matching x address.

Claims 1-3, 9, 13-15, 21, 24-27, and 33 stand rejected under 35 U.S.C. § 103(a) as obvious over U.S. Patent No. 3,551,895 ("Driscoll"); with Manuel Alfonseca,

Object-Oriented Programming Tutorial, and Jacques Cohen, *A View of the Origins and Development of PROLOG*, cited as extrinsic evidence. Claims 4-6, 16-18, and 28-30 stand rejected under § 103(a) as obvious over Driscoll and David J. Lilja ("Lilja"), *Reducing the Branch Penalty in Pipelined Processors*. Claims 10, 22, and 34 stand rejected under § 103(a) as obvious over Driscoll and the appellants' admitted prior art ("AAPA"). Claims 11 and 23 stand rejected under § 103(a) as obvious over Driscoll and U.S. Patent No. 5,615,386 ("Amerson").

II. OPINION

Our opinion addresses the rejections in the following order:

- Examiner's rejections
- Board's rejection.

A. EXAMINER'S REJECTIONS

"Rather than reiterate the positions of the examiner or the appellants *in toto*, we focus on the point of contention therebetween." *Ex parte Muresan*, No. 2004-1621, 2005 WL 951659, at *1 (Bd.Pat.App & Int. Feb 10, 2005). To wit, the examiner asserts, "as can be seen in column 2, lines 45-50 of Driscoll, the advance branch instruction is placed at some point ahead of the actual branch instruction. Therefore, since the actual branch instruction has not yet been reached, the advance branch instruction is

necessarily independent of a specific currently pending branch instruction."

(Examiner's Answer at 11.) The appellants make the following argument.

> [T]he "advance branch instruction" of Driscoll is dependent on an upcoming (i.e., pending) branch instruction. By its very name, the Driscoll "advance branch instruction" refers to a related branch instruction. Because Driscoll's advance branch instruction is paired with a branch instruction, the advance branch instruction can not be independent of a currently pending branch instruction, i.e., there is a relationship between the two.

(Reply Br. at 4.) In addressing the point of contention, the Board conducts a two-step analysis. First, we construe the independent claims at issue to determine their scope. Second, we determine whether the construed claims would have been obvious.

1. Claim Construction

"Analysis begins with a key legal question — *what* is the invention *claimed*?" *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561, 1567, 1 USPQ2d 1593, 1597 (Fed. Cir. 1987). Here, independent claim 1 recites in pertinent part the following limitations: "executing said update prefetch stream instruction to load at least one address pair into a set associative array of x,y address pairs, wherein the at least one address pair is **independent of a specific currently pending branch instruction**. . . ." (Emphasis added.) Independent claims 13 and 25 include similar limitations.

2. Obviousness Determination

"Having determined what subject matter is being claimed, the next inquiry is whether the subject matter would have been obvious." *Ex Parte Massingill*, No. 2003-0506, 2004 WL 1646421, at *3 (Bd.Pat.App & Int. May 20, 2004). "In rejecting claims under 35 U.S.C. Section 103, the examiner bears the initial burden of presenting a *prima facie* case of obviousness." *In re Rijckaert*, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993) (citing *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992)). "'A *prima facie* case of obviousness is established when the teachings from the prior art itself would appear to have suggested the claimed subject matter to a person of ordinary skill in the art.'" *In re Bell*, 991 F.2d 781, 783, 26 USPQ2d 1529, 1531 (Fed. Cir. 1993) (quoting *In re Rinehart*, 531 F.2d 1048, 1051, 189 USPQ 143, 147 (CCPA 1976)).

Here, Driscoll discloses "a computer look-ahead branch detecting system. . . ." Col. 4, ll. 6-7. "The system utilizes a special Advance Branch Instruction which will be located in an instruction sequence a number of positions prior to the actual potential branch point. It specifies the point at which the branch is to be taken if conditions require and also the point to which the branch is to go." Col. 1, ll. 14-19. More specifically, a "'From' field contains the address of the instruction after which the branch is perhaps to be made, and the 'To' field the address of the instruction to be executed if

the branch is successful (i.e., it corresponds to the 'Branch Address' of an ordinary branch instruction)." Col. 4, ll. 58-63.

Although "the 'Advance Branch' instruction must appear at least four steps before the pont to which it refers," col. 6, ll. 13-15, we are unpersuaded that such a location makes "the advance branch instruction . . . necessarily independent of a specific currently pending branch instruction." (Examiner's Answer at 11.) To the contrary, because the advance branch instruction refers to "the instruction after which the branch is perhaps to be made," col. 4, ll.59-60, and "the address of the instruction to be executed if the branch is successful," *id.* at ll. 61-62, a dependency exists between the advance branch instruction and the "paired . . . branch instruction." (Reply Br. at 4.)

Furthermore, the examiner does not allege, let alone show, that the addition of Lilja, AAPA, or Amerson cures the aforementioned deficiency of Driscoll. Absent a teaching or suggestion of the aforementioned limitations, we are unpersuaded of a *prima facie* case of obviousness. Therefore, we reverse the obviousness rejections of claims 1, 13, and 25, and of claims 2-6, 9-11, 14-18, 21-24, 26-30, 33, and 34, which depend therefrom.

B. BOARD'S REJECTION

Under 37 C.F.R. § 41.50(b)(2005), we enter a new ground of rejection against claims 1-6, 9-11, 13-18, 21-30, 33, and 34, i.e., all the pending claims. "[C]ompliance with the 'written description' requirement of §112 is a question of fact. . . ." *Vas-Cath, Inc. v. Mahurkar*, 935 F.2d 1555, 1563, 19 USPQ2d 1111, 1116 (Fed. Cir. 1991) (citing *In re Gosteli*, 872 F.2d 1008, 1012, 10 USPQ2d 1614, 1618 (Fed. Cir. 1989); *Utter v. Hiraga*, 845 F.2d 993, 998, 6 USPQ2d 1709, 1714 (Fed. Cir. 1988)). "'Although [the applicant] does not have to describe exactly the subject matter claimed, . . . the description must clearly allow persons of ordinary skill in the art to recognize that [he or she] invented what is claimed.'" 935 F.2d at 1563, 19 USPQ2d at 1116 (quoting *Gosteli*, 872 F.2d at 1012, 10 USPQ2d at 1618). "[T]he test for sufficiency of support . . . is whether the disclosure of the application relied upon 'reasonably conveys to the artisan that the inventor had possession at that time of the later claimed subject matter.'" *Ralston Purina Co. v. Far-Mar-Co., Inc.,* 772 F.2d 1570, 1575, 227 USPQ 177, 179 (Fed. Cir. 1985) (quoting *In re Kaslow*, 707 F.2d 1366, 1375, 217 USPQ 1089, 1096 (Fed. Cir. 1983)). "Application sufficiency under §112, first paragraph, must be judged as of the filing date [of the application]." *Vas-Cath*, 935 F.2d at 1566, 19 USPQ2d at 1119 (citing *United States Steel Corp. v. Phillips Petroleum Co.*, 865 F.2d 1247, 1251, 9 USPQ2d 1461, 1464 (Fed. Cir. 1989)).

Here, as aforementioned, independent claims 1, 13, and 25 recite the limitation that "the at least one address pair is independent of a specific currently pending branch instruction." The limitation is not an original limitation; it was added by an amendment. (Paper No. 4.) "[W]hen filing an amendment an applicant should show support in the original disclosure for new or amended claims." M.P.E.P. § 2163.II.A.3(b) (8th ed., rev. 1, Feb. 2003).[1] When they filed the aforementioned amendment, however, the appellants neglected to show support in the original disclosure for the amended claims.[2] For our part, we are unable to find support for the limitation that "the at least one address pair is independent of a specific currently pending branch instruction." Therefore, we reject claims 1, 13, and 25; and claims 2-6, 9-11, 14-18, 21-24, 26-30, 33, and 34, which depend therefrom; under 35 U.S.C. § 112, ¶ 1, as lacking a written description.

III. CONCLUSION

In summary, the rejections of claims 1-6, 9-11, 13-18, 21-30, 33, and 34 under § 103(a) are reversed. A new rejection of the same claims under § 112, ¶ 1, is added. 37 C.F.R. § 41.50(b) provides that "[a] new grounds of rejection pursuant to this

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[1]We cite to the version of the M.P.E.P. in effect at the time of the amendment.

[2]Of course, it is not too late for the appellants to show such support.

paragraph shall not be considered final for judicial review." Section 41.50(b) also provides that, within two months from the date of the decision, the appellant must exercise one of the following options to avoid termination of proceedings of the rejected claims:

> (1) Submit an appropriate amendment of the claims so rejected or new evidence relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the proceeding will be remanded to the examiner. . . .
>
> (2) Request that the proceeding be reheard under 37 C.F.R. § 41.52 by the Board upon the same record. . . .

No time for taking any action connected with this appeal may be extended under 37 C.F.R. § 1.136(a).

REVERSED
37 C.F.R. § 41.50(b)

KENNETH W. HAIRSTON	)	
Administrative Patent Judge	)	
	)	
	)	
	)	
	)	BOARD OF PATENT
JERRY SMITH	)	APPEALS

Administrative Patent Judge	)	AND
	)	INTERFERENCES
	)	
	)	
	)	
LANCE LEONARD BARRY	)	
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