

The opinion in support of the decision being entered today was *not* written with publication in mind and is *not* binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte Synopsis, Inc.¹

Appeal No. 2005-2512
Reexamination Control No. 90/006,431
Patent 5,872,952²

ON BRIEF

Before MARTIN, JERRY SMITH, and CRAWFORD, Administrative Patent Judges.

MARTIN, Administrative Patent Judge.

DECISION ON APPEAL

¹ The owner of record of the patent under reexamination.

² Issued February 16, 1999, based on Application 08/424,876, filed April 17, 1995. The inventors named in the '952 patent are Jeh-Fu Tuan and Peiqi He. Peiqi He's name was later changed to Patrick Ho. See Ho's October 22, 2003, "Declaration of Inventor Regarding RailMill and ChipViewer" ("First Ho Declaration") par. 1.

This is an appeal under 35 U.S.C. §§ 134 and 305 from the examiner's final rejection of claims 1-18, which are all of the claims subject to reexamination, under 35 U.S.C. §§ 112 (first paragraph), 102, and 103. The examiner has withdrawn the § 112 rejection, Ans. 3,³ leaving only the art rejections for our consideration.

We affirm in part and reverse in part.

A. The real party in interest

The real party in interest is the current patent owner, Synopsys, Inc., of Mt. View, California ("Synopsys"). In 1997, Synopsys acquired the original assignee, i.e., EPIC Design Technology, Inc. of Santa Clara, California (hereinafter "Epic"), and the '876 application, which matured into the '952 patent. Br. 11; PTO assignment records.

This reexamination proceeding was initiated at the request of Nassda Corporation ("Nassda").

B. Related reexamination proceeding

³ The final Office action (Paper No. 31), brief, answer, and reply brief are hereinafter abbreviated "Fin.Act.," "Br.," "Ans.," and "R.Br."

A “Notice of Related Reexamination Proceeding”⁴ filed in this reexamination proceeding by the Patent Owner (Synopsis) explains that Patent 5,878,053, which is the subject of Reexamination Control No. 90/006,331 (also requested by Nassda), is related to the ‘952 patent involved in this reexamination proceeding. Nassda’s request for reexamination of the ‘053 patent (“‘053 Request”) identifies two litigations involving that patent: Synopsis, Inc. v. Nassda Corporation, Case No. C-01-2519 SI (N.D. Cal, San Francisco Division); and Synopsis, Inc. v. An-Chang Deng, et al., Case No. CV 787950 (Santa Clara County Superior Court, Cal.). ‘053 Request 2-3. An-Chang Deng is a founder and an officer of Nassda. Id. at 3. The ‘053 Request states that “due to a procedural defense asserted by Synopsis, Nassda is foreclosed from challenging the validity of the ‘053 patent in court. Accordingly, the U.S. Patent and Trademark Office (“Patent Office”) is the only forum in which these substantial new questions of patentability can be addressed or resolved.” Id. at 2-3.

Appellant contends that the outcome of neither reexamination proceeding should have any effect on the other because the inventions claimed in the two involved patents are significantly different. Br. 4.

On April 18, 2006, the PTO issued a reexamination certificate in the ‘331 reexamination proceeding confirming the patentability of some claims of the ‘053 patent and canceling others.

⁴ Paper No. 10, dated March 21, 2003.

C. Appellant's claimed invention

The "Background" portion of the '952 patent explains that the invention "relates to computer-aided design (CAD) tools for analyzing integrated circuits and, more particularly, to analyzing power Vdd and ground nets in integrated circuits for electromigration, voltage drop and ground bounce." '952 Patent, col. 1, ll. 20-24. The term "power net" refers to the wire connections between the power Vdd or ground pads and the circuit elements. Id. at col. 3, ll. 47-50. The "Background" portion contrasts the invention with known CAD tools as follows:

Numerous CAD tools exist for simulating transistor networks of ICs (e.g., SPICE).^[5] An innovative system is described in U.S. patent application Ser. No. 08/040,531 [now Patent 5,446,676], entitled "Transistor-Level Timing and Power Simulator and Power Analyzer", filed Mar. 29, 1993 by Huang et al., and U.S. patent application Ser. No. 08/231,207 [abandoned], entitled "Power Diagnosis for VLSI Designs", filed Apr. 21, 1994 by An-Chang Deng, which are both hereby incorporated by reference for all purposes. However, none of the prior art systems allow the user to simulate the power nets of an IC and display

⁵ As explained in one of the references relied on by the examiner, SPICE is a copyright of the Board of Regents, University of California, Berkeley. See Archer Systems, Inc., ARCADIA User Manual, Version 1.1 (Feb. 1995) ("Arcadia Manual") at iii.

power net characteristics like voltage drop, current density and ground bounce. The present invention fulfills this and other needs.

Id. at col. 1, l. 61 to col. 2, l. 6. As explained below, the preferred embodiment of the invention employs a “DRACULA®” system available from Cadence Design Systems, Inc. (Cadence”), an “ARCADIA” system available from Archer Systems, Inc. (“Archer”), and a “ChipViewer product” which is not described as being available from a vendor.

Figure 1 of the ‘952 Patent, which depicts a preferred embodiment of the invention, is reproduced below:

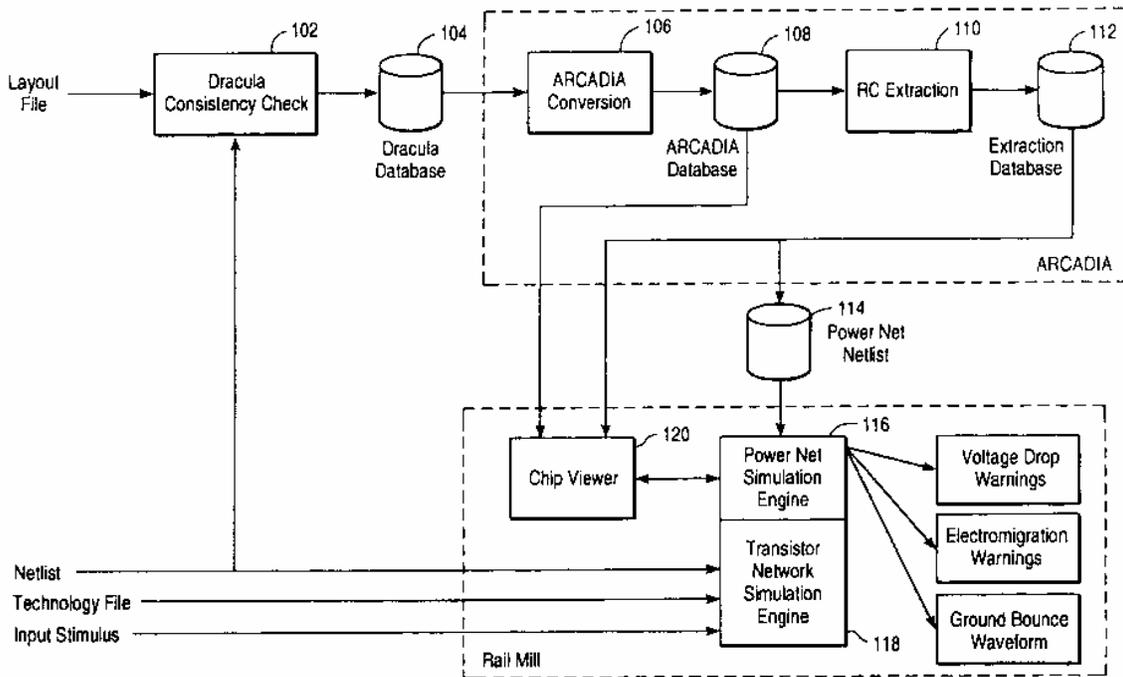


FIG. 1

“In a preferred embodiment, the power net simulation engine [116] of the present invention operates in conjunction with a transistor network (i.e., circuit) circuit simulation engine [118].” ‘952 Patent, col. 3, ll. 27-30. These two simulation engines and ChipViewer 120 are shown contained within the dashed-line block labeled “Rail Mill,” a term which does not appear in the ‘952 patent specification but appears in some of the cited references in descriptions of a “RailMill™” product available from Epic.

The transistor network simulation engine 118 in the “Rail Mill” block is described as based on the “PowerMill” simulation product available from Epic and described in Application 08/040,531 (now Patent 5,446,676), which is incorporated by reference in the ‘952 patent. Id. at col. 4, ll. 35-43.⁶ It is therefore evident that PowerMill predates RailMill. The transistor network simulation engine

simulates the circuit operation according to the input stimulus file and specified power supply voltages. The transistor network simulation engine generates the current drawn by the circuit devices, including the circuit devices connected to the power net. The transistor network simulation may utilize constant power supply voltages or the power supply voltages calculated by the power net simulation.

Id. at col. 4, ll. 44-51.⁷

⁶ PowerMill is described in the Deng reference as a transistor-level power simulator and analyzer providing the following functions: (1) accurate power estimation; (2) DC leakage path detection; (3) short-circuit transient leakage estimation; (4) hot-spot detection; and (5) power diagnosis. Deng at 3.

⁷ The transistor network simulation engine receives three input files: The netlist file defines the circuit to be simulated and is constructed

from circuit elements connected by input and output nodes to form a network. A circuit element can be a single transistor, resistor, capacitor, gate, register, functional model, and the like. . . . The wire connections between elements are referred to as "nets." . . .

The technology file is a data file containing user-specified MOS parameters and SPICE generated characteristics (i.e., Vgs, Vds v. Ids). The input stimulus file contains input data used to stimulate the simulated circuit.

'952 Patent, col. 3, ll. 42-53 (emphasis added).

The power net simulation engine 116 is responsive to a power net netlist 114, which is a list of the wire connections between the power (Vdd) or ground pads and the circuit elements. Id. at col. 3, ll. 47-50. In the Figure 1 embodiment, the power net netlist is extracted from an RC extraction database 112 generated by an ARCADIA system from Archer, id. at col. 4, ll. 18-22, which is responsive to a DRACULA® database 104 generated by a DRACULA® integrated circuit layout verification system available from Cadence. Id. at col. 4, ll. 8-12. Alternatively, the power net netlist can be provided by “other power net netlist extractors including power net netlist extractors.” Id. at col. 4, ll. 23-32.

The power net simulation engine 116 “uses the current information [from transistor network simulation engine 118] to calculate the voltage drop and current in the branches of the power net. The power net simulation engine generates voltage drop, electromigration and ground bounce warnings during simulation.” Id. at col. 4, ll. 51-54. The specification explains that “the present invention provides a ChipViewer product that displays power net characteristics to the user.” Id. at col. 12, ll. 30-32. During simulation, highlight computer files containing information about the voltage drop or current density characteristics of the power net are read by the ChipViewer product, which utilizes the highlight files in conjunction with the extracted power net netlist file to display characteristics of the power net. Id. at col. 13, ll. 13-19. The ChipViewer displays the different values for voltage drop and current density in different colors on the layout so as to allow the user to quickly identify areas of interest. Id. at col. 4, ll. 56-

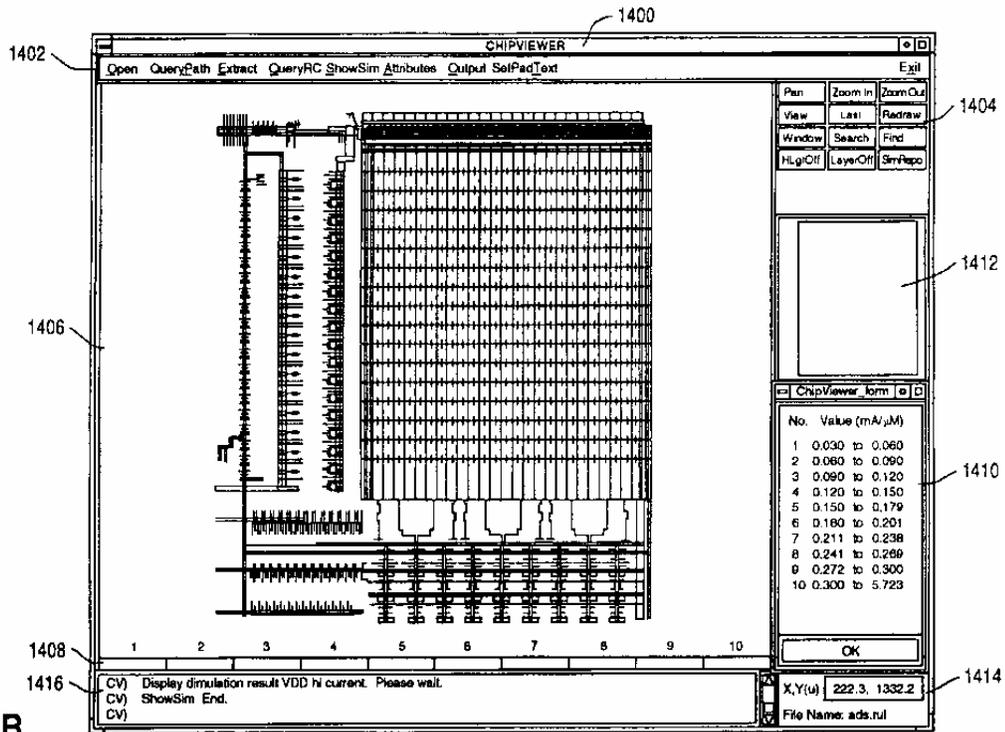


FIG. 14B

60. The ChipViewer additionally allows the user to zoom in on specific areas of the power net or query to determine specific values. Id. at col. 4, ll. 61-63. Two ChipViewer display screens are depicted in Figures 14A and 14B, which respectively show the voltage drop characteristics and the current density characteristics of a power net. Figure 14B of the '952 Patent is reproduced below:

When a user utilizes the zoom-in button of display buttons 1404, a rectangle appears in reference window 1412 to identify the location of the portion of the chip layout which is currently being displayed in the chip layout display window 1406. Id. at col. 12, ll. 53-60.

D. The claims

The first Office action⁸ included rejections of claims 1-18 over prior art. In the “Response to First Official Action,”⁹ appellant amended all of the independent claims (i.e., claims 1 and 16-18) to more specifically recite a “graphical user interface including interactive tools for viewing selected portions of said power net.” Claim 17 thus amended, which is one of the broader independent claims, reads on the Figure 1 embodiment as follows:¹⁰

17. (amended). A system for analyzing power nets of an integrated circuit, comprising:
a power net extractor [ARCADIA], said power net extractor extracting a power net netlist [114] for a power net from an integrated circuit layout;
a circuit simulator [118] coupled to said power net extractor, said circuit simulator determining current at selected integrated circuit devices of said integrated circuit electrically connected to said power net;
a power net simulator [116] coupled to said circuit simulator, said power net simulator determining a characteristic of portions of said power net according to current at said selected integrated circuit devices; and

⁸ Paper No. 14, mailed August 25, 2003.

⁹ Paper No. 17, received October 24, 2003.

¹⁰ The discussions of the rejections in the Final Office Action quote the claims in their original, unamended form. However, the examiner states at page 57 thereof that the amendments have been considered.

a display [ChipViewer 120] coupled to said power net simulator, said display displaying a graphical user interface including a layout representation of said power net, the graphical user interface including interactive tools for viewing selected portions of said power net, the layout representation of said power net including said characteristic of said selected portions of said power net.

E. The references

The references relied on in the rejections are:¹¹

Mitsuhashi	U.S. 5,404,310	Apr. 4, 1995
Rusu	U.S. 5,598,348	Jan. 28, 1997 (filed Sep. 22, 1994)

Archer Systems, Inc., "ARCADIA User Manual -- Advanced RC Analysis and DIAGnostic Program," Version 1.1 (Feb. 1995), Chapters 1-7 ("Arcadia Manual").

"RailMill™ Product Brief," Epic Design Technology (undated) ("RailMill PB").

"RailMill™ – Improving Reliability in Deep Submicron ICs" (undated) ("RailMill IR"), Epic Design Technology (undated).

"Chapter 2 – RailMill Tutorial," Epic Design Technology (Mar. 24, 1995) ("RailMill Tutorial").¹²

¹¹ The examiner has withdrawn his reliance on two additional references: (a) Huang U.S. Patent 5,446,676; and (b) Rugen, et al. "An interactive layout design system with real-time logical verification and extraction of layout parasitics" (June 1988). Ans. 3.

¹² RailMill PB, RailMill IR, and RailMill Tutorial are hereinafter collectively referred to as "the RailMill documents."

An-Chang Deng, "Power Analysis For CMOS/BiCMOS Circuits, Workshop Proceedings, International Workshop on Lower-Power Design, pp. 3-8 (Apr. 1994) ("Deng").

T. Noguchi, K. Hatanaka, and K. Maeguchi, "A Threshold Pulse Width for Electromigration Under Pulsed Stress Conditions," June 12-13, 1989 VMIC Conference, VLSI Multilevel Interconnection Conference, 1989 Proceedings, Sixth International IEEE, pp. 183-89 ("Noguchi").

Don Stark, "Analysis of power supply networks in VLSI circuits," PhD dissertation, Stanford University (1991) ("Stark").¹³

Gyanendra Tiwary, "Below the half-micron mark," IEEE Spectrum, pp. 84-87 (Nov. 1994) ("Tiwary").

F. The grounds of rejection

The grounds of rejection, as modified to reflect the examiner's withdrawal of his reliance on Huang and Rugen, are as follows:¹⁴

(1) Claims 1-18 stand rejected under § 102(a) as anticipated by "RailMill" as disclosed in the three RailMill documents, which the examiner considers to be "one

¹³ The initial twelve pages of the version of Stark of record are out of order and the abstract is on an unnumbered sixth page. Also, Figures 80-85 at pages 124-29 are not clear. Clearer copies of pages 124-29 have been downloaded from http://www-visi.stanford.edu/papers/ds_thesis.pdf and accompany this decision, as does a copy of cover page i, which in the downloaded version contains the abstract.

¹⁴ As noted by appellant, the examiner is incorrect to hold that claims 1-18 stand or fall together under 37 CFR § 1.192(c) for lack of a statement in the brief that they do not stand or fall together. Ans. 3 para. 7. That provision was replaced effective September 13, 2004, by 37 CFR § 41.37(c), which does not include such a requirement. Rules of Practice Before the Board of Patent Appeals and Interferences; Final Rule, 69 Fed. Reg. 49,960, 49,960, 50,006 (Aug. 12, 2004); reprinted in 1286 Off. Gaz. Pat. & Trademark Office 21, 21, 59-60 (Sep. 7, 2004).

teaching,” citing MPEP § 2131.01 (“Multiple Reference 35 U.S.C. 102 Rejections”).

Fin.Act. 9.

(2) Claims 1-6, 9, and 16-18 stand rejected under § 102(a) as anticipated by Stark. Fin.Act. 10 para. 19. However, the Answer restates the basis of the rejection as § 102(b). Ans. 4.

(3) Claims 1-6, 9, and 16-18 stand rejected under § 103(a) for obviousness over Stark in view of the Arcadia Manual, Tiwary, or Deng. Fin.Act. 20 para. 25.

(4) Claims 1-6, 9, and 16-18 stand rejected under § 103(a) over Rusu in view of the Arcadia Manual, Tiwary, or Deng. Fin.Act. 29 para. 37.

(5) Claims 7 and 8 stand rejected under § 103(a) over either one of Stark and Rusu considered in view of Railmill PB and RailMill IR. Fin.Act. 31 para. 47.

(6) Claims 10 and 11 stand rejected under § 103(a) over either one of Stark and Rusu considered in view of the Railmill documents. Fin.Act. 33 para. 53.

(7) Claims 10 and 11 stand rejected under § 103(a) over either one of Stark and Rusu considered in view of any one of the Arcadia Manual, Tiwary, and Deng and further in view of Noguchi. Fin.Act. 33 para. 54.

(8) Claims 12-15 stand rejected under § 103(a) over either of Stark and Rusu in view of the Railmill documents. Fin.Act. 35 para. 67.

(9) Claims 1-6, 9, and 16-18 stand rejected under § 103(a) over the Arcadia Manual in view of Railmill PB or Mitsuhashi. Fin.Act. 37 para. 72.

(10) Claims 7 and 8 stand rejected under § 103(a) over the Arcadia Manual in view of the Railmill documents. Fin.Act. 39 para. 78.

(11) Claims 10 and 11 stand rejected under § 103(a) over the Arcadia Manual in view of the Railmill documents. Fin.Act. 41 para. 84

(12) Claims 10 and 11 stand rejected under § 103(a) over the Arcadia Manual in view of Mitsuhashi and further in view of Noguchi. Fin.Act. 42 para. 90.

(13) Claims 12-15 stand rejected under § 103(a) over the Arcadia Manual in view of the RailMill documents. Fin.Act. 43 para. 95.

One of the principal questions before us, which affects all of the rejections except the § 102(b) rejection based on Stark, is whether and to what extent the RailMill documents, the Arcadia Manual, Tiwary, and Deng are available as printed publications under 35 U.S.C. § 102(a), as argued by the examiner. Appellant makes two arguments. The first, which applies to all six documents, is that the Ho declarations establish that the subject matter relied on by the examiner in these documents was invented by Ho and Tuan and thus is not available as prior art against appellant's claims under § 102(a). Br. 21. See In re Katz, 687 F.2d 450, 454, 215 USPQ 14, 17 (CCPA 1982) ("a printed publication cannot stand as a reference under §102(a) unless it is describing the work of another"); see also MPEP § 716.10 (8th ed. rev. 4, Oct. 2005) (discussing Rule 132 affidavits of the "attribution" type).

Regarding the three RailMill documents (but not the Arcadia Manual, Tiwary, or Deng), appellant alternatively argues that the documents have not been shown to have publication dates prior to appellant's April 17, 1995, filing date.

G. The merits of appellant's argument that the RailMill documents are not printed publications having publication dates prior to appellant's filing date

The burden of proof on the question of whether the RailMill documents are printed publications and were published prior to appellant's April 17, 1995, filing date rests on the examiner. Cf. In re Hall, 781 F.2d 897, 899, 228 USPQ 453, 455 (Fed. Cir. 1986):

The proponent of the publication bar must show that prior to the critical date the reference was sufficiently accessible, at least to the public interested in the art, so that such a one by examining the reference could make the claimed invention without further research or experimentation. See In re Donohue, 766 F.2d 531, 533, 226 USPQ 619, 621 (Fed. Cir. 1985); In re Bayer, 568 F.2d at 1361, 196 USPQ at 674; In re Wyer, 655 F.2d [221,] 226-27, 210 USPQ [790,] 794-95 [(CCPA 1981)].

The statutory phrase "printed publication" has been interpreted to mean that before the critical date the reference must have been "disseminated or otherwise made available to the extent that persons interested and ordinarily skilled in the subject matter or art exercising reasonable diligence, can locate it and recognize and comprehend therefrom the essentials of the claimed invention without need of further research or experimentation." Bruckelmyer v. Ground Heaters, Inc., 445 F.3d 1374, 1378, 78 USPQ2d 1684, 1687 (Fed. Cir. 2006) (quoting Wyer, 655 F.2d at 226, 210 USPQ at 795).

The examiner argues that "U.S. Patent 5,828,580 refers to Arcadia (col. 4, lines 9-17); said patent was filed on 11/8/1995; this indicates that RailMill was also available

before 11/8/1994 (See In re Epstein, 32 F.3d 1559, 1564, 31 USPQ2d 1817, 1820 (Fed. Cir. 1994)).”

Fin.Act. 8 para. 18. This argument confuses the status of the RailMill documents as prior printed publications, whose contents can be relied on to reject claims under reexamination, with their status as evidence of prior public knowledge or use of the RailMill product, which knowledge or use is not a proper basis for rejecting claims under reexamination. See 37 CFR § 1.552:

§ 1.552 Scope of reexamination in ex parte reexamination proceedings.

(a) Claims in an ex parte reexamination proceeding will be examined on the basis of patents or printed publications and, with respect to subject matter added or deleted in the reexamination proceeding, on the basis of the requirements of 35 U.S.C. 112.

(b) Claims in an ex parte reexamination proceeding will not be permitted to enlarge the scope of the claims of the patent.

(c) Issues other than those indicated in paragraphs (a) and (b) of this section will not be resolved in a reexamination proceeding. . . .

See also MPEP § 2258, subsection I, part B (“A rejection on prior public use or sale, insufficiency of disclosure, etc., cannot be made even if it relies on a prior art patent or printed publication.”). In Epstein, the court did not consider or approve of relying on product release dates to establish publication dates, as the examiner is asking us to do. Instead, the court approved of the board’s reliance on product release dates given in subsequently published abstracts to establish that the products were placed on sale on those release dates.

As further evidence that the RailMill documents were published prior to appellant’s April 17, 1995, filing date, the examiner contends that because the

Arcadia Manual discloses the same RailMill product that is disclosed in the RailMill documents, the February 1995 publication date of the Arcadia Manual (which appellant has not challenged) must be assumed to apply as well to the RailMill documents.

Fin.Act. 9. The fact that the Arcadia Manual was published prior to appellant's filing date does not establish that any of the RailMill documents relied on as prior art were published prior to that date. The same criticism applies to the examiner's reliance on the fact that page 16 (as numbered at the bottoms of the pages by appellant) of the source code appendix to the '952 patent shows a copyright date of 1992 and includes the following RailMill code segment: "if (strcmp (programe, "railmill")) return 1[.]"

Ans. 18-19.

We also agree with appellant that the examiner is incorrect to treat the three RailMill documents in the § 102 rejection based thereon as "one teaching," in support of which he cites MPEP § 2131.01 ("Multiple Reference 35 U.S.C. 102 Rejections").

Fin.Act. 9. In the Final Action, the examiner explained that "each one [of the RailMill documents] refers to the earliest version of RailMill which as noted (See Arcadia, discussed earlier) . . . was publicly available by at least 11/1994." Id. This argument is unpersuasive for the reasons given above in the discussion of the examiner's reliance on Epstein. In the Answer, the examiner gave the alternative explanation that the three documents "each show inherent features in greater detail than may have been disclosed in the other," Ans. 18, which is one of the three justifications given in MPEP §

2131.01 for basing a § 102 rejection on multiple references.¹⁵ This argument fails for lack of an explanation of which subject matter in which document is being relied on to prove that the same subject matter is necessarily present in another document. To the extent the examiner is contending that the RailMill documents as a group show all of the features that were inherent in a RailMill product that was publicly known or used prior to appellant's filing date, the argument fails because, as already noted, a rejection in a reexamination proceeding cannot properly be based on the public knowledge or use provisions of § 102(a) .

For the foregoing reasons, we will treat the § 102(a) rejection which is based on the RailMill documents as being based on those documents in the alternative.

Our analysis of the publication dates of the RailMill documents is as follows.

1. RailMill PB

¹⁵ The other reasons are to prove that the primary reference contains an enabled disclosure and to explain the meaning of a term used in the primary reference. MPEP § 2131.01.

While this document does not show any date, the earliest possible publication date can be deduced from the fact that the bottom of the last page explains that the “Arcadia” trademark is owned by Epic. In contrast, the Arcadia Manual, dated February 1995, identifies Archer as the owner of the “Arcadia” mark. As a result, the date of RailMill PB is necessarily subsequent to the date Epic acquired Archer, which appears to have been subsequent to May 22, 1995, which is after appellant’s April 17, 1995, filing date. Specifically, at page 62, paragraph 175, of the final Office action, the examiner cites the following article as evidence that Archer was acquired by Epic after May 22, 1995: “EPIC Design Tech to acquire Archer [S]ystems in stock swap,” Electronic News (May 22, 1995). Nor is an earlier date asserted in the only declaration testimony of record which addresses that question. The declaration by Deng entitled “Declaration of Prior Art Publication Date” (“Deng Declaration”), which accompanied the Patent Owner’s “Prior Art Citation Pursuant to 37 C.F.R. 1.555,”¹⁶ explains that the printing date of RailMill PB is believed to be “prior to” December 1995 without specifying an earlier date. Deng Decl. para. 5. RailMill PB therefore has not been demonstrated to have a publication date prior to appellant’s April 17, 1995, filing date.

¹⁶ Paper No. 9, received March 19, 2003.

2. RailMill IR

The last line of the last page (Bates No. S0016075) of this is document shows a date of “7/2/96,” thereby establishing that this document was not published prior to appellant’s filing date.

3. RailMill Tutorial

The cover page of this document reads:

Chapter 2
RailMill Tutorial
March 24, 1995

The other chapter or chapters of the source document are not part of the record.¹⁷ The March 24, 1995, date is prior to appellant’s filing date. That this document was intended for use by members of the interested public is apparent from the second page thereof (S0059875), which explains: “This chapter provides a step-by-step process to get you started using RailMill and to teach you the key steps involved before and in running a RailMill simulation.” Furthermore, the “RailMill Installation” discussion at the same page explains, “You should have set your path to access the RailMill and Arcadia executables and have licenses to run them.” However, these facts are not sufficient to prima facie establish that prior to appellant’s April 17, 1995, filing date, RailMill Tutorial was actually “disseminated or otherwise made available to the extent that persons interested and ordinarily skilled in the subject matter or art exercising reasonable diligence, can locate

¹⁷ At page S0059881, RailMill Tutorial refers to “the Arcadia chapter” without giving the chapter number.

it and recognize and comprehend therefrom the essentials of the claimed invention without need of further research or experimentation.” Bruckelmyer, 445 F.3d at 1378, 78 USPQ2d at 1687; Wyer, 655 F.2d at 226, 210 USPQ at 795. As the record does not include any evidence establishing when, if ever, RailMill Tutorial was disseminated or otherwise made available to persons skilled in the art, it has not been shown to be available as a prior-art printed publication against appellant’s claims.

4. Summary

None of the RailMill documents has been shown to be available as a prior-art printed

publication against appellant’s claims.

H. Whether any of the subject matter in the RailMill documents, the Arcadia Manual, Tiwary, and Deng has been established to be the invention of Ho and Tuan

In the interest of completeness, this analysis assumes that the RailMill documents have

publication dates prior to appellant’s filing date, as do the Arcadia Manual, Tiwary, and Deng.

In order to remove reference subject as prior art on the ground it represents the applicant’s own invention, the applicant (or patent owner during reexamination) must prove invention and derivation of that subject matter. See In re Facius, 408 F.2d 1396, 1407, 161 USPQ 294, 302 (CCPA 1969) (“The real question is whether, in addition to establishing derivation of the relevant disclosure from himself, appellant has

also clearly established the fact that he invented the relevant subject matter disclosed in the patent.”). Furthermore, an uncontradicted “unequivocal statement” from the applicant regarding the subject matter disclosed in an article, patent, or published application will be accepted as establishing inventorship. In re DeBaun, 687 F.2d 459, 463, 214 USPQ 933, 936_(CCPA 1982).

The First Ho Declaration was filed with the “Response to First Official Action.”¹⁸ That declaration credits Ho and Tuan with “develop[ing] products known as RailMill, and integrat[ing] the RailMill product with an interactive graphical user interface known as ChipViewer.” First Ho. Decl. para. 2. Insofar as ChipViewer is concerned, the examiner understood this testimony to mean that Ho and Tuan used ChipViewer to view the RailMill outputs rather than that they invented ChipViewer per se. Second Office Action 66.

Paragraphs 4 and 5 of the declaration assert that the to the extent the RailMill document and the Arcadia Manual refer to “RailMill and the use of ChipViewer to display the output from RailMill,” they describe “our invention, and the work of our team at Epic Design Technology, Inc.” First Ho Declaration paras. 4-5. The examiner criticized the “our team” language as creating an ambiguity regarding who invented the subject matter relied on in the references. Second Office Action 65. The examiner also

¹⁸ Paper No. 17, received October 24, 2003.

criticized the First Ho Declaration because it is not signed by both inventors. Second Office Action 65.

Appellant's "Response to Second Official Action"¹⁹ was accompanied by a "Second Declaration by Inventor" (hereinafter "Second Ho Declaration"). As correctly noted by appellant at page 23 of that response, MPEP § 716.10 does not require that all inventors sign an attribution declaration. In any event, the absence of a signature or supporting declaration by Tuan is adequately addressed at pages 13-14 of the brief, which explain that Tuan is one of the founders of and is employed by Nassda, the third-party requestor, which party as noted above is also a litigation opponent. As will appear, the "our team" language which the examiner found objectionable in the First Ho Declaration does not appear in the Second Ho Declaration.

We will begin by determining the meaning of the term "RailMill" as used in the Second Ho Declaration. As already noted, the block labeled "Rail Mill" in Figure 1 of the '952 patent includes transistor network simulation engine 116, power net simulation engine 118, and also ChipViewer 120. That designation is consistent with the RailMill documents, issued by Epic, which describe the RailMill product as including all three of

¹⁹ Papert No. 29, received July 7, 2004.

these components. For example, in RailMill PB the display feature is among the features listed in RailMill PB, which explains that the RailMill product:

- Accurately extracts the power/ground network from the IC layout.
- Simulates the IC design at the transistor level to determine current flow throughout the power network.
- Displays the power network layout and overlays electromigration and voltage drop information on the display to clearly show where problems exist.
- Allows “what-if” analysis to determine corrective actions to eliminate problems before fabricating silicon.

RailMill PB at 1. The caption for Figure 3 further explains that the display function is provided by ChipViewer:

RailMill reads LVS database and extracts the power net for analysis. A power net simulation engine and a transistor simulation engine determine where electromigration and voltage drop

may exist in the
design. A layout
display and query
tool called
ChipViewer shows
the relationship of
simulation results to
the power network
layout.

RailMill PB at 4.

The Second Ho Declaration, on the other hand, appears to treat ChipViewer as separate from “RailMill,” explaining that the integrated combination of RailMill and ChipViewer was released as Archer’s “Arcadia” product:

2. The invention that became the ‘952 patent was conceived and reduced to practice in the United States while my co-inventor and I were employed by Epic Design Technology. As part of reducing to practice the invention of the ‘952 Patent, my work was directed to combining an interactive graphical user interface with power network analysis tools then being developed primarily by my co-inventor. Moreover as part of this reduction to practice, Epic Design Technology, in collaboration with Archer Systems, integrated Epic’s RailMill product with the graphical user interface known as ChipViewer. The RailMill product with the graphical user interface referred to as ChipViewer was then released as the Arcadia product. The RailMill and ChipViewer parts of Arcadia are therefore our own reduction to practice of the invention conceived by my co-inventor and I as claimed in the ‘952 Patent.

Second Ho Decl. para. 2 (emphasis added).²⁰ The same distinction between RailMill and ChipViewer's use therewith is observed in paragraphs 4 and 5 of the Second Ho Declaration, which discuss the Arcadia Manual and the RailMill documents, respectively:

4. . . . [T]o the extent that the [Arcadia Manual] document refers to RailMill and the use of ChipViewer to display the outputs from RailMill, it describes our own implementation of the invention.

5. . . . [T]o the extent that those [RailMill] documents describe RailMill and the use of ChipViewer to display the outputs from RailMill, they describe an embodiment of our invention, made by us.

Second Ho Decl. paras 4-5. Consequently, we understand the term "RailMill" as used in this declaration to refer to the power net simulation engine and associated transistor network simulation engine but not ChipViewer. Furthermore, insofar as ChipViewer is concerned, we do not understand that testimony to mean that Ho and Tuan invented ChipViewer per se. Rather, it can reasonably be understood to mean that they used an existing ChipViewer product (presumably with some modification) to display the voltage drop and current information in the manner depicted in Figures 14A and 14B,

²⁰ Because a Rule 131 attribution declaration is offered to prove inventorship (i.e., conception) and derivation of the subject matter relied on in the reference, it is not necessary to consider the merits of the assertions of a reduction to practice.

respectively, of the '952 patent. Had Ho intended to credit himself and Tuan with the invention of ChipViewer per se, his paragraph 4 and 5 testimony should have asserted that to the extent the RailMill documents describe RailMill and ChipViewer, they describe an embodiment of their invention. Appellant is therefore incorrect to characterize Ho's testimony as establishing that Ho and Tuan invented "both ChipViewer and ChipViewer integrated with RailMill," R.Br. 14, and to assert that "the inventors herein are responsible for ChipViewer." Br. 12. Moreover, as explained below, that position appears be contrary to other evidence of record, including the Arcadia Manual.

We will first, however, consider Ho's testimony vis-à-vis the RailMill documents. We begin by noting it is evident from the details given in the RailMill documents that they are directed to the same power net simulation engine, associated transistor network simulation engine, and use of ChipViewer to display the output of the power net simulation engine that are disclosed and claimed the '952 patent. For example, the RailMill Tutorial discusses the steps of (a) converting the Dracula database to Arcadia (see p. S0059876), (b) performing RC extraction (S00569880), (c) creating a power net netlist (S0059881), and (d) running the RailMill simulations to obtain images representing electromigration, voltage drop, and power grids (S0059882-85).²¹ Also, the "ShowSim" software discussed at pages S0059883-85 of the RailMill Tutorial

²¹ The RailMill Tutorial also explains that all of these functions are controlled using ChipViewer.

corresponds to the “showsim.c” software module which is mentioned in the ‘952 patent at column 14, line 65, and reproduced at pages 30-44 of the software appendix to that patent, noted as column 14, lines 60-65.

The examiner nevertheless questions Ho’s above-quoted testimony that “to the extent [the RailMill] documents describe RailMill and the use of ChipViewer to display the outputs from RailMill, they describe an embodiment of our invention, made by us,” Second Ho Decl. para. 5, on several grounds, none of which are persuasive. The first, which is apparently offered in response to appellant’s contention that Ho and Tuan invented ChipViewer per se, is that that argument is contradicted by other evidence of record, including the Arcadia Manual, which the examiner construes as attributing the invention of ChipViewer to Archer rather than Epic personnel. Ans. 9 (quoting paragraph 175 of the Final Action). As support for refusing to give weight to the declaration under these circumstances, the examiner cites Ex parte Kroger, 219 USPQ 370, 371-72 (Bd. Pat. App. 1982), which is cited in MPEP § 716.10. Ans. 9-11 para. 178. Kroger held that declarations by applicants Kroger and Rod alleging that they invented the subject matter relied on in a reference article co-authored by Kroger and Knaster were unpersuasive because they were contradicted by other evidence of record, namely, a letter by Knaster asserting co-inventorship of that subject matter with Kroger and Rod and evidence of Knaster’s refusal to sign a supporting declaration. Although for the reasons given below we agree with the examiner that the Arcadia Manual appears to credit ChipViewer per se to

Archer rather Epic personnel, that does not contradict Ho's testimony, which insofar as ChipViewer is concerned credits Ho and Tuan only with using ChipViewer to display the RailMill outputs.

The examiner's alternative argument that the declaration testimony is contradicted by the above-noted ongoing litigation (Ans. 12) is not understood and will not be further addressed, except to note that that litigation involves the aforementioned '053 patent rather than the '952 patent, which is under reexamination in this proceeding.

The examiner also contends that Ho's testimony is insufficient to remove the RailMill documents as prior art in the absence of a supporting declaration by the authors of those documents. Those documents fail to name any authors and Ho testified that he does not know their identities. See Second Ho Decl. para. 5 ("The [RailMill] documents attached hereto as Exhibits B-D describe RailMill as well. I do not know who the actual authors of the documents are"). As support for this position, the examiner cites a decision by the Director of Technology Center (TC) 2100 on a petition appellant filed in response to a requirement for information²² issued by the examiner. "Response to Petition Under 37 C.F.R. § 1.59" (hereinafter "Petition Decision").²³ The Petition Decision, in addition to modifying the examiner's requirement for information in ways not

²² Second Office Action at 1-9.

²³ Paper No. 25, mailed June 4, 2004.

relevant to this appeal, commented on the First Ho Declaration as follows (the Second Ho Declaration is not addressed):

The declaration makes the following assertions:

- (a) The invention was made when appellants were at Epic Design;
- (b) Declarant and co-inventor created RailMill and integrated RailMill and ChipViewer; and
- (c) Arcadia manual produced by Archer [S]ystems[:] “to the extent these documents describe [refer to] RailMill and the use of ChipViewer to display the outputs from RailMill, they [it] describe[s] our invention, and the work of our team at Epic...”.

Note that statement (c) is conclusory in nature with no evidence or statement of facts to support it. Furthermore, there is no claim or explanation of derivation or attribution on the part of the authors/publishers of the references.

In any event, Patrick Ho has admitted that ChipViewer was not his invention and that he is not the author of the Arcadia Manual or the RailMill documents. Patent Owner amended his claims to be limited to (1) RailMill and the (2) integration of RailMill and ChipViewer, which is what Patrick Ho identifies in the declaration as his invention.

Petition Decision at 4 (emphasis added). The TC Director’s conclusion that the First Ho Declaration is insufficient to prove derivation or attribution in the absence of supporting declarations by the (unnamed) authors or by the publishers of the RailMill documents is not binding on the examiner or this Board, because, in our view, that conclusion concerns the substantive merits of the declaration and thus is outside the scope of a TC Director’s authority regarding Rule 132 affidavits and declarations, which is limited “to [their] formal sufficiency and propriety.” MPEP § 1002.02(c), item 3(c). Nor do we find ourselves in agreement with the merits of the TC Director’s position, which is not supported in the Petition Decision by the citation of any decisional authority.

Furthermore, while the examiner (Ans. 9-11) quotes extensively from MPEP § 716.10, which discusses a number of cases involving Rule 132 declarations, he does not explain which case he believes provides support for such a requirement. We have, however, considered Katz, which is the most recent Federal Circuit decision to address the merits of a Rule 132 attribution showing, and for the reasons given below fail to see how it supports such a requirement.

Katz involved a rejected under 35 U.S.C. § 102(a) for anticipation by an article which “fully describes the claimed invention,” Katz, 687 F.2d at 452, 215 USPQ at 15, and named as coauthors the sole applicant (Katz) and two other individuals. The board affirmed the examiner’s holding that Katz’s Rule 132 declaration was insufficient in the absence of supporting declarations from the other coauthors. Id. at 453, 215 USPQ at 16. The court began its analysis by explaining that a determination of whether an article raises a substantial question of inventorship depends not only on its authorship but on its content, nature, and circumstances of publication:

As an initial matter, we hold that authorship of an article by itself does not raise a presumption of inventorship with respect to the subject matter disclosed in the article. Thus, co-authors may not be presumed to be coinventors merely from the fact of co-authorship. On the other hand, when the PTO is aware of a printed publication, which describes the subject matter of the claimed invention and is published before an application is filed (the only date of invention on which it must act in the absence of other proof), the article may or may not raise a substantial question whether the applicant is the inventor. For example, if the author (whether he is the applicant or not) specifically states that he is describing the work of the applicant, no question at all is raised. The content and nature of the printed publication, as well as the circumstances surrounding its publication, not merely its authorship, must be considered.

Id. at 455, 215 USPQ at 18. The court held that the article created a substantial question of inventorship because the research work disclosed therein, which was the same subject matter disclosed and claimed in the application, was described as the work of all of the authors:

What we have in this case is ambiguity created by the printed publication. The article does not tell us anything specific about inventorship, and appellant is only one of three authors who are reporting on scientific work in which they have all been engaged in some capacity at the Harvard Medical School. It was incumbent, therefore, on appellant to provide a satisfactory showing which would lead to a reasonable conclusion that he is the sole inventor.

Katz, 687 F.2d at 455, 215 USPQ at 18 (emphasis added; footnote omitted). Despite its conclusion that the article raised a question of inventorship, the court did not require supporting declarations by Katz's coauthors. Instead, the court considered it sufficient that Katz's Rule 132 declaration (a) "reaverred . . . that he is the inventor of the subject matter described and claimed in his application and also that disclosed in the [reference article]," id., and (b) explained that his coauthors were students who were working under his direction and supervision. Id. The Katz court was thus not presented with, and did not address, the question of whether supporting declarations would have been required if the reference article had named no authors.

The examiner's underlying concern may be that Ho, not being an author of the RailMill documents, lacks first-hand knowledge of facts to support his testimony that the subject matter in those documents was derived from him and Tuan. We do not agree.

That testimony, though conclusory, is clearly supported by the similarities between the subject matter disclosed in the RailMill documents and the subject matter disclosed and claimed in the '952 patent. While Ho's declaration preferably should have explained that his conclusory testimony is based on those similarities, such an explanation is not required where, as here, the testimony finds clear support in those similarities. It is also significant that Ho's testimony regarding inventorship of the RailMill subject matter does not conflict with (1) the RailMill documents themselves, which do not name any authors, let alone appear to attribute the disclosed subject matter to the authors, as in Katz, or (2) any other evidence of record regarding inventorship, as in Kroger.

For the foregoing reasons, we hold that the Second Ho Declaration is sufficient to establish that to the extent the RailMill documents disclose the RailMill power net simulation engine, associated transistor network simulation engine, and use of ChipViewer to display the output of the power net simulation engine (which is virtually all of the subject matter disclosed in those documents), they are not prior art with respect to appellant's claims.

2. The Arcadia Manual

While the Arcadia Manual includes subject matter like that present in the RailMill documents, it also differs from those documents in several significant respects. First, it was published by Archer rather than by Epic. Second, at page iii it identifies ChipViewer as a copyright of Archer, which as of the February 1995 publication date had not been acquired by Epic, and at page 7-1 describes ChipViewer as “the Graphical User Interface to ARCADIA.” Third, the Arcadia Manual discloses ChipViewer being used with simulators other than RailMill. Thus, Figure 1-3 (at page 1-8), reproduced below, shows ARCADIA being used to generate netlists for SPICE, TimeMill, PowerMill, or RailMill, of which the last three are identified at page iii as Epic simulators:

F

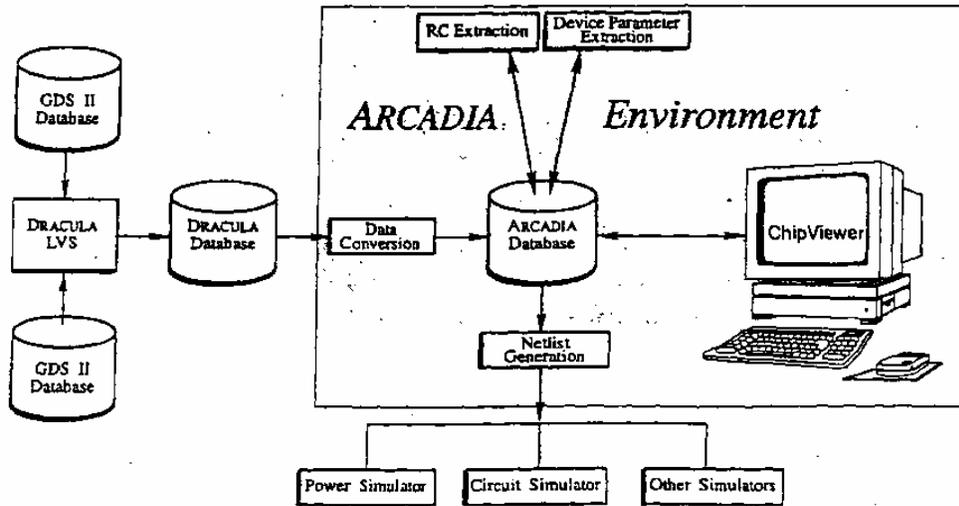


Figure 1-1: ARCADIA uses existing data to provide accurate netlists.

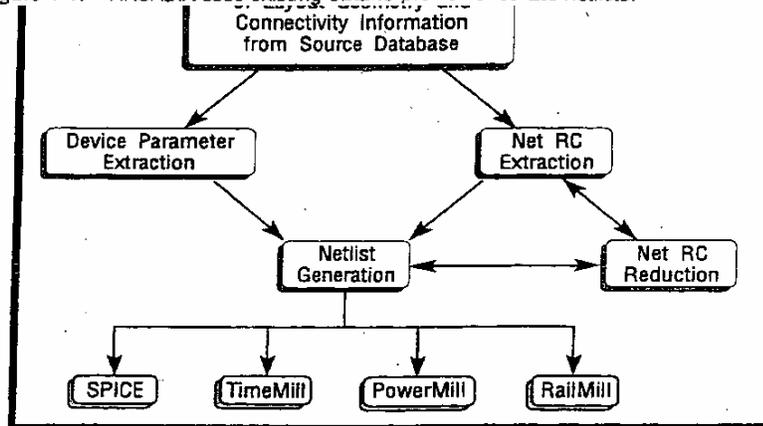


Figure 1-3: Steps in using ARCADIA function to generate a netlist.

Furthermore, Figure 1-1, at page 1-1 (i.e., Chapter 1, page 1) and

reproduced below, depicts ChipViewer as part of the ARCADIA environment rather than as part of a particular simulator.

As explained at page 7-1, which does not indicate that the discussion is specific to RailMill, the ChipViewer graphical user interface consists of:

- Operation Menu (control)
- Display Controls (control)
- Reference Window (information)
- Layer Attribute Controls (control)
- Chip Layout Display Window (information and control)
- Cursor Coordinate Window (control)
- Console Window (information)

Also, although most of Chapter 7 (“ChipViewer”) discusses using ChipViewer to display RailMill simulations, it also discusses PowerMill at page 7-9, wherein it explains that a PowerMill simulation yields a display of the dynamic current, voltage, and power distributions.

However, to the extent the Arcadia Manual discloses the RailMill power net simulation engine, associated transistor network simulation engine, and use of ChipViewer to display the RailMill output information, it discloses the same subject matter that is disclosed and claimed in the ‘952 patent. For example, the “ShowSim” software that is credited by the Arcadia Manual (at page 7-7) with “open[ing] an interactive link to RailMill” corresponds to module “showsim.c” at pages 30-44 of the software Appendix to the ‘952 patent. Therefore, for reasons like those given above in the discussion of the RailMill documents we hold that Ho’s testimony is sufficient to

remove the Arcadia Manual as prior art to the extent it discloses the RailMill power net simulation engine and associated transistor network simulation engine and the use of ChipViewer to display the RailMill output information.²⁴

Regarding the fact that Arcadia Manual was issued by Archer rather than by Epic, which issued the RailMill documents, that circumstance is adequately explained by Ho's testimony that "Epic Design Technology, in collaboration with Archer Systems, integrated Epic's RailMill product with the graphical user interface known as ChipViewer. The RailMill product with the graphical user interface referred to as

²⁴ As noted earlier, Ho testified:

4. The actual authors of the Arcadia User Manual attached hereto as Exhibit A, by Archer Systems, Inc., are not known to me. However, to the extent that the document refers to RailMill and the use of ChipViewer to display the outputs from RailMill, it describes our own implementation of the invention.

Second Ho Decl. para. 4

ChipViewer was then released as the Arcadia product.” Second Ho Decl. para. 2.
Kroger is inapposite because the Arcadia Manual does not contradict Ho’s testimony that he and Tuan invented RailMill and the use of ChipViewer to display the RailMill outputs.

Our holding that Ho’s testimony is sufficient to remove the Arcadia Manual only to the extent it discloses the RailMill power net simulation engine and associated transistor network simulation engine and the use of ChipViewer to display the RailMill output information means that the Arcadia Manual is still prior art under § 102(a) in all other respects, including its disclosure of using ChipViewer with simulators other than RailMill, namely, SPICE, PowerMill, and TimeMill. Because Ho’s declaration fails to explain which display features of ChipViewer, if any, were invented by him and Tuan in order to display the RailMill outputs, we must assume that they not invent any of the following ChipViewer features described at page 1-3 and reproduced below, which are not described therein as limited to RailMill:

- Graphical point-and-click operation
- Visual navigation through the layout to explore any area of the chip layout
- Full zoom and pan capability
- Numerical evaluation of the details of a selected net by extracting accurate interconnect model parameters
- Analyze model parameters using a time domain simulator

Arcadia Manual at p. 1-3 (emphasis added). Treating these ChipViewer display features as not limited to RailMill is also consistent with the ‘580 patent, filed November 8, 1994, on which (as noted above) the examiner unsuccessfully relied to attribute that

date to the RailMill documents.²⁵ That patent, which appellant correctly notes refers to ARCADIA at column 4, line 13, and to ChipViewer in numerous places, Br. 24, makes no mention of RailMill or voltage drop simulations yet discusses ChipViewer's zoom feature at column 4, lines 59-60.

For the foregoing reasons, we hold that the Arcadia Manual is available as prior art under 35 U.S.C. § 102(a) with respect to appellant's claims to the extent it discloses using ChipViewer as a graphical user interface for circuit analysis simulators other than RailMill, such as PowerMill, and more particularly for its disclosure that ChipViewer as used with those other simulators permits the display the characteristics of selected portions of the circuitry.

²⁵ Neither of the inventors of the '952 patent under reexamination is named as an inventor in the '580 patent, which is assigned to Epic.

3. Tiwary and Deng

Tiwary at page 87 explains that the author is a senior applications engineer at Epic. The caption for Figure 3 describes it as a display generated by PowerMill, a power management tool for detecting dc paths and other sources of power drain. Figure 3 is not described as depicting a ChipViewer display and does not resemble the RailMill ChipViewer displays depicted in Figures 14A and 14B of the '952 patent. Figure 4, on the other hand, closely resembles Figure 14A of the '952 patent and is accompanied by the following caption: "Voltage drops in a static RAM power net are made apparent by being displayed in different colors for different ranges of values. Color and voltage range keys are at the bottom and the lower right. Power supply inputs are at the left, top and bottom." Tiwary also explains:

So, in deep submicron designs, voltage drop analysis is crucial [Fig. 4].

One way to perform power-net simulation is to divide a design into two parts—a standard transistor circuit and a power network of extracted supply voltage and ground nets. The transistor current information is computed (assuming a constant supply voltage) and passed on to the power-net simulator. The node voltages and branch currents thus obtained can be used for checking voltage drops. Peak voltage drops can be checked against user-specified thresholds. This gives designers a quick way of identifying problem areas in their designs.

Tiwary 86 (brackets in original). Tiwary does not, however, mention RailMill.

The Deng article at page 3 likewise identifies its author as an employee of Epic. The features of the PowerMill product are discussed at pages 3-7. At page 7, Deng discusses a proposed two-step method for performing a power-net simulation:

A two-step method has been proposed. In the first step, PowerMill is applied to find currents flowing into the transistor blocks. PowerMill assumes constant voltages at power buses during this step. Step two simulates the power-bus network, modeled as an RLC network and driven by current sources representing the simulated currents in step one. Based on this scheme, a power-net reliability simulation package is being developed and tested. It includes a layout extractor to model the power net in terms of the extracted RLC parasitics, a power-net simulator to simulate the RLC network driven by current sources estimated from PowerMill simulation on the transistor blocks, and a layout display tool to highlight the excessive current densities and voltage drops in the power net. Figure 2 shows the voltage drop distribution in the power net. Although the actual display separates voltage levels by color, they can be distinguished here by shades of gray.

Deng at 7, cols. 1, 2 (footnote omitted). The image depicted in Figure 2 at page 7 closely resembles an image in the RailMill ChipViewer display depicted by Figure 14B of the '952 patent, more particularly the image in chip layout display window 1406 of the display. Deng, like Tiwary, makes no mention of RailMill.

Ho's only discussion of the content of Tiwary and Deng is as follows:

6. . . . The Tiwary document describes work of Epic Design Technology. I am informed that the Examiner has referred to page 86, where images of a graphical user interface are shown. Because I have never seen this article before, and was not consulted in the preparation of the article, I do not know the origin of the images on page 86. However, the images on page 86 appear to have been generated using ChipViewer.

7. . . . The [Deng] article describes the PowerMill product of Epic Design Technology. I am informed that the Examiner has referred to Figure 2, on page 7 of the article. Because I have never seen this article before, and was not consulted in the preparation of the article, I do not know the origin of the image in Figure 2. However, the image in Figure 2 appears to have been generated using ChipViewer.

Second Ho Decl. paras. 6-7. Even assuming for the sake of argument that Ho is correct to conclude that the images appearing at page 86 of Tiwary (i.e., Figures 3 and 4) and the image in Figure 2 of Deng were generated using ChipViewer, that fact is insufficient to remove those images or their associated descriptions as prior art, because neither Ho nor any other witness has testified that these ChipViewer images represent the outputs generated by RailMill, i.e., by Ho and Tuan's power-net simulation engine.²⁶ Appellant has therefore failed to establish that the subject matter relied on in Tiwary and Deng was invented by Ho and Tuan and thus does not constitute prior art. However, as explained below, for other reasons the rejections are being reversed to the extent they are based on these references.

I. The effect of the foregoing holdings on the grounds of rejection

In view of the foregoing holdings, we are reversing the rejections to the extent they rely on (a) any of the RailMill documents or (b) the Arcadia Manual to the extent it discloses the RailMill power net simulation engine and associated transistor network simulation engine and the use of ChipViewer to display RailMill information. Therefore, the only grounds of rejection left for our consideration are the rejections of:

- (a) Claims 1-6, 9, and 16-18 under § 102(b) for anticipation by Stark;

²⁶ Because it is not evident from an inspection of Tiwary and Deng that the images in question depict ChipViewer images produced using RailMill, any testimony to that effect by Ho would have been unpersuasive in the absence of an explanation of the factual basis for such testimony.

(b) Claims 1-6, 9, and 16-18 under § 103(a) for obviousness over Stark in view of the
the
Arcadia Manual (excluding RailMill and the associated use of ChipViewer), Tiwary, or
Deng;

(c) Claims 1-6, 9, and 16-18 under § 103(a) over Rusu in view of the Arcadia
Manual (excluding RailMill and the associated use of ChipViewer), Tiwary, or Deng;
and

(d) Claims 10 and 11 under § 103(a) over either of Stark and Rusu considered in
view of any of the Arcadia Manual (excluding RailMill and associated use of
ChipViewer), Tiwary, and Deng, and further considered in view of Noguchi.

J. The rejection of claims 1-6, 9, and 16-18 under § 102(b) for anticipation by Stark

The Stark abstract explains that the document is a thesis which “describes *Ariel*, a CAD tool that helps VLSI designers analyze power supply noise. The system consists of three main components, a resistance extractor, a current estimator, and a linear solver, that are used together to determine the voltage drops and current density along the supply lines.” Stark abstract, 2d para. Figures 80-85 of Stark, at pages 124-29, are displays showing the results of the voltage drop and current calculations. In Figure 80, for example, dots that are completely black represent nodes where the voltage drop is half a volt or more. Stark 120. As indicated by the voltage scale at the left of that figure, smaller voltage drops are represented by corresponding shades of gray. Id.

Taking claim 17 as representative,²⁷ appellant does not deny that Stark discloses the claimed power net extractor “for extracting a power net netlist for a power net from an integrated circuit layout,” a circuit simulator coupled to said power net extractor for “determining current at selected integrated circuit devices of said integrated circuit electrically connected to said power net,” and a power net simulator for “determining a characteristic of portions of said power net according to current at said selected integrated circuit devices.”²⁸ Nor does appellant deny that Stark’s Figures 80-85 are generated by a display which is “coupled to the power net simulator” and “display[s] a layout representation of said power net including said characteristic of portions of said power net,” as required by claim 17 before amendment. Instead, appellant denies that Stark satisfies the “graphical user interface” limitations added by that amendment, which in claim 17 call for the recited display to “display[] a graphical user interface including a

²⁷ See 37 CFR § 41.37(c)(vii) (“When multiple claims subject to the same ground of rejection are argued as a group by appellant, the Board may select a single claim from the group of claims that are argued together to decide the appeal with respect to the group of claims as to the ground of rejection on the basis of the selected claim alone.”).

²⁸ The examiner reads the limitations of claim 17 prior amendment onto Stark at pages 16-18 of the Final Office Action.

layout representation of said power net, the graphical user interface including interactive tools for viewing selected portions of said power net, the layout representation of said power net including said characteristic of said selected portions of said power net.” Br. 25-26 (emphasis added).

The examiner and appellant disagree about whether Stark discloses a “graphical user interface” at all, let alone one that satisfies the remaining claim limitations. Claims under reexamination must be given their broadest reasonable interpretations consistent with the specification. In re Hyatt, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000) (citing In re Graves, 69 F.3d 1147, 1152, 36 USPQ2d 1697, 1701 (Fed. Cir. 1995); In re Etter, 756 F.2d 852, 858, 225 USPQ 1, 5 (Fed. Cir. 1985) (en banc)). Inasmuch as the term is not defined in the ‘952 patent and no definition has been provided by the examiner or appellant, we hereby adopt the following definition of the term: “A type of display format that enables the user to choose commands, start programs, and see files and other options by pointing to pictorial representations (icons) and lists of menu items on the screen. Choices can generally be activated either with the keyboard or with a mouse.” Microsoft Press Computer Dictionary 185 (2d ed. 1994) (copy enclosed). None of the displays depicted in Figures 80-85 of Stark fit this description, as no user-selectable menus or icons are shown. Instead, the figures are graphical representations of the analyzed circuits in which different magnitudes of the voltage drops and current densities are depicted as respective shades of gray or black. Furthermore, these figures fail to reveal any means for viewing selected portions of the

power net, as also required by the claim. Instead, each figure depicts the entire circuit under analysis.

The examiner is incorrect to argue that a graphical user interface is inherently present because “Stark discloses that the package that the disclosure in the Theses is implemented on ‘Ariel’, which is a CAD [computer-aided design] package.” Second Office Action 51 para. 115 (adhered to in Fin.Act. 49, para. 118; Ans. 21). As appellant correctly notes, “Ariel” is the name Stark gives to his disclosed analysis tool and is an acronym of “Analyzer for Resistance and current (I) ELelements.” Stark 2 & n.1. It is not a graphical user interface.

The rejection of claim 17 under § 102(b) for anticipation by Stark is therefore reversed. Because the other independent claims (i.e., claims 1, 16, and 18) recite similar limitations, we are also reversing the § 102(b) rejection of claims 1-6, 9, 16, and 18 on that ground.

K. The rejection of claims 1-6, 9, and 16-18 under § 103(a) for obviousness over Stark in view of the Arcadia Manual (excluding RailMill and associated use of ChipViewer), Tiwary, or Deng

Appellant does not deny that Stark satisfies all of the limitations of the independent claims as they stood prior to being amended to specify that the recited “display” displays “a graphical user interface including interactive tools for viewing selected portions of said power net.”²⁹ The examiner contends it would have been obvious in view of the Arcadia Manual, Tiwary, or Deng to use a graphical user interface to display the results of Stark’s power net simulation. Fin.Act. 20 paras. 27 29, 30, 32, 33. As explained above, we are considering the Arcadia Manual only to the extent it does not disclose RailMill and the use of ChipViewer to display the RailMill outputs.

²⁹ The examiner’s explanation of how claim 17 prior to amendment reads on Stark appears at pages 26-28 of the Final Office Action.

Considering first the Arcadia Manual, as evidence of motivation the examiner cites page 1-1 and more particularly the assertion that visualization of modern VLSI/ULSI chips consisting of millions of devices is a critical factor in successful circuit design and the description of ChipViewer as providing fast visualization of the IC or any part of the IC. Fin.Act. 21 para. 33. We agree with this reasoning to the extent it is based on the Arcadia Manual's disclosure of using ChipViewer with simulators other than RailMill. Furthermore, as noted above, ChipViewer as used with these other simulators appears to include the zoom feature, which permits display of selected portions of the circuitry under analysis, as required by the claims. Appellant's sole argument against relying on the Arcadia Manual's disclosure of ChipViewer is that ChipViewer per se is not prior art (Br. 28; R.Br. 23³⁰), which argument fails to recognize that ChipViewer is disclosed in the Arcadia Manual as being useful with simulators other than RailMill. The rejection of claim 17 for obviousness over Stark in view of Arcadia Manual is therefore affirmed, as is the rejection on this ground of claims 1-6, 9, 16, and 18, which are not separately argued. 37 CFR § 41.37(c)(vii).

However, the rejection is reversed to the extent it is alternatively based on Deng or Tiwary. While those references disclose using what appears to be graphical user interfaces for displaying the outputs of simulators, including a PowerMill simulator and power-net simulators under development, the examiner has not explained why, nor is it

³⁰ Reference to pages of the reply brief are to the page numbers at the bottom of the pages.

apparent, why these references would have been understood to suggest using a graphical user interface which can display selected portions of the power net, as required by the claims. The record copy of Tiwary's Figure 4, which is the figure in Deng and Tiwary that most resembles Figure 14A of the '952 patent, lacks sufficient clarity to determine what, if any, display options are available.³¹

We note in passing that appellant's argument that Tiwary and Deng are not enabling insofar as the graphical user interface is concerned is not entitled to consideration because it was raised for the first time in the reply brief, at 23-25.

Thus, the rejection of claims 1-6, 9, and 16-18 of claims 1-6, 9, and 16-18 for obviousness over Stark in view of the Arcadia Manual, Tiwary, or Deng is affirmed to the extent based on Stark in view of the Arcadia Manual (excluding RailMill and associated use of ChipViewer) and reversed to the extent based on Stark in view of Tiwary or Deng.

³¹ The PTO's Scientific & Technical Information Center (STIC) was unable to supply a clearer copy of Tiwary.

L. The rejection of Claims 1-6, 9, and 16-18 under § 103(a) over Rusu in view of the Arcadia Manual (excluding RailMill and associated use of ChipViewer), Tiwary, or Deng

Rusu discloses a method and apparatus to model the power network of a VLSI circuit. The method includes the step of extracting the power network associated with a semiconductor circuit layout and then deriving a compacted power network from the power network. Rusu, col. 2, ll. 18-22. The operation of the compacted power network is simulated on a circuit simulation program to identify areas in the compacted power network that do not comply with predetermined power network performance criteria, such as electromigration limits and voltage drop limits. Id. at col. 2, ll. 34-39.

Appellant does not deny that Rusu discloses all of the limitations recited in claim 17 apart from the graphical user interface limitations, for which the examiner relies on Arcadia Manual, Tiwary, or Deng. The examiner's reliance on the ChipViewer in the Arcadia Manual is convincing in this rejection for the same reasons that are given in above in the discussion of the § 103 rejection in which Stark is the primary reference. Furthermore, his reliance on Tiwary and Deng is unconvincing for the reasons given that discussion. Appellant's criticism of the proposed combination of teachings of Rusu and the Arcadia Manual on the ground that ChipViewer is not available as prior art, Br. 29-30, is unavailing for the reasons noted above.

Accordingly, the rejection of claims 1-6, 9, and 16-18 for obviousness over Rusu in view of Arcadia Manual is affirmed to the extent based on Rusu in view of the Arcadia

Manual (excluding RailMill and associated use of ChipViewer) and reversed to the extent based on Rusu in view of Tiwary or Deng.

M. The rejection of Claims 10 and 11 under § 103(a) over either of Stark and Rusu in view of any of the Arcadia Manual (excluding RailMill disclosures), Tiwary, and Deng and further in view of Noguchi

Appellant does not separately argue the merits of claims 10 and 11, instead arguing that they are allowable for the same reasons as claim 1, on which they depend through claim 9. Br. 32-33. The rejection of claims 10 and 11 is therefore affirmed for the reasons given above for affirming the rejections of claims 1 and 9 based on either of Stark and Rusu considered in view of the Arcadia Manual (excluding RailMill and associated use of ChipViewer). 37 CFR § 41.37(c)(vii).

N. Summary

The only grounds of rejection which we have affirmed are:

(a) The rejection of claims 1-6, 9, and 16-18 under § 103(a) for obviousness over Stark in view of the Arcadia Manual (excluding RailMill disclosures);

(b) The rejection of claims 1-6, 9, and 16-18 under § 103(a) over Rusu in view of the Arcadia Manual (excluding RailMill disclosures); and

(c) The rejection of claims 10 and 11 under § 103(a) over either of Stark and Rusu in view of the Arcadia Manual (excluding RailMill disclosures) and further in view of Noguchi.

All of the rejections of dependent claims 7, 8, and 12-15 are reversed.

O. Extensions of time

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR 1.136(a). See 37 CFR §§ 41.50(f) and 41.52(b).

AFFIRMED-IN-PART; REVERSED-IN-PART

JOHN C. MARTIN)	
Administrative Patent Judge)	
)	
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)	BOARD OF PATENT
JERRY SMITH)	APPEALS AND
Administrative Patent Judge)	INTERFERENCES
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)	
MURRIEL E. CRAWFORD)	
Administrative Patent Judge)	

Appeal No. 2005-2512
Reexamination Control No. 90/006,431

JCM/jcm/mg

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cc:

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Enclosures:

- (1) Microsoft Press Computer Dictionary 185 (2d ed. 1994).
- (2) Cover sheet and pages 124-29 of Stark thesis downloaded from http://www-visi.stanford.edu/papers/ds_thesis.pdf.