

The opinion in support of the decision being entered today was *not* written for publication and is *not* binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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*Ex parte* SANJAY RAGHUNATH DESHPANDE, PETER STEVEN  
LENK, and MICHAEL JOHN MAYFIELD

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Appeal 2006-0016  
Application 10/347,536  
Technology Center 2100

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Decided: June 8, 2007

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Before LANCE LEONARD BARRY, HOWARD B. BLANKENSHIP, and  
ALLEN R. MACDONALD, *Administrative Patent Judges*.

BARRY, *Administrative Patent Judge*.

DECISION ON APPEAL

I. STATEMENT OF THE CASE

A Patent Examiner rejected claims 37-48 and 60-65. The Appellants appealed therefrom under 35 U.S.C. § 134(a). To assist us in deciding their appeal, we ordered the Appellants to "map[ ] each of the claimed limitations

to specific pages and lines of the specification and reference characters of the drawings. . . ." *Ex parte Deshpande*, No. 2006-0016, at 3 (B.P.A.I. 2006).

The Appellants responded by merely citing those pages and lines of their specification that presumably relate to each claim. (Supp. Appeal Br. 5-8.) They failed, however, to address the mapping of **each limitation** of the claims. Nor did they map anything to the drawings.

Furthermore, the Appellants' citations were broad. Regarding claim 37, for example, they cited "page 54, line 16, through page 67, line 3, and more particularly page 60, line 26, through page 61, line 18," (*id.* 5), of their specification. Such citations have proven of minimal assistance in deciding their appeal. We **choose** not to dismiss the instant appeal at this time, nevertheless, and will endeavor to map the limitations to specific pages and lines of the specification and to reference characters of their drawings as best as we can.

#### A. INVENTION

The invention at issue on appeal is a "distributed system structure for a large-way, multi-bus, multiprocessor system using a bus-based cache-coherence protocol." (Specification 4.) According to the Appellants, symmetric multiprocessing systems have been designed around a common bus to which all processors and devices are connected. The common bus serves as the pathway for transferring commands and data between the

processors and devices and for achieving coherence among the system's cache and memory. (*Id.* at 1.)

The single-system-bus design also simplified the task of achieving coherence among the system's caches. (*Id.*) More specifically, the Appellants recognize two broad classes of cache-coherence protocols, viz., bus-based snooping protocols and directory-based protocols. (*Id.* 2.) Although a single-system-bus design is currently preferred for implementing coherence protocol, the Appellants assert that "it cannot be employed for a large-way multiprocessor system." (*Id.* 3.)

In contrast, the Appellants' invention organizes master devices into a set of nodes supported by a node controller. The node controller receives and queues commands received from master device and communicates therewith. A bus protocol "reports the state of a cache line to a master device along with the first beat of data delivery for a cacheable coherent Read." (*Id.* 4.) "[T]he node controller helps to maintain cache coherency for commands by blocking a master device from receiving certain transactions so as to prevent Read-Read deadlocks." (*Id.*)

Claim 37, which further illustrates the invention, follows.

37. A method of maintaining cache coherency by prohibiting Read-Read deadlocks in a multiprocessor system, the method comprising the steps of:

requesting a Read transaction of a cache line by a processor;

attempting, simultaneously by multiple processors including said processor, to gain ownership of said cache line;

in response to receiving, by said processor, a coherency response indicating state information for data to be read by the Read transaction will be delivered along with delivery of the data, abstaining, by said processor, from going critical by blocking transactions that collide with said Read transaction from being received by said processor during processing of said Read transaction, said processor and said other processors being prohibited from gaining ownership of said cache line during said processing of said Read transaction, wherein Read-Read deadlocks are prohibited.

## B. REJECTIONS

Claims 37-48 and 60-65 stand rejected under 35 U.S.C. § 112, ¶ 1, as lacking a written description. Claims 37-40, 42-48, 60-63, and 65 stand rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 5,297,269 ("Donaldson"). Claims 38-48 and 61-65 stand rejected under 35 U.S.C. § 103(a) as obvious over Donaldson and U.S. Patent No. 6,330,643 ("Arimilli").

## II. WRITTEN DESCRIPTION REJECTION

"[T]o assure separate review by the Board of individual claims within each group of claims subject to a common ground of rejection, an appellant's brief to the Board must contain a clear statement for each rejection:

(a) asserting that the patentability of claims within the group of claims subject to this rejection do not stand or fall together, and (b) identifying which individual claim or claims within the group are separately patentable and the reasons why the examiner's rejection should not be sustained." *In re*

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*McDaniel*, 293 F.3d 1379, 1383, 63 USPQ2d 1462, 1465 (Fed. Cir. 2002) (citing 37 C.F.R. §1.192(c)(7)(2001)). "If the brief fails to meet either requirement, the Board is free to select a single claim from each group of claims subject to a common ground of rejection as representative of all claims in that group and to decide the appeal of that rejection based solely on the selected representative claim." *Id.*, *Id.*

Here, the Appellants stipulate, "For the purposes of this appeal, claims 37-48 and 60-65 stand or fall together as one group." (Br. 4.) We select claim 37 as the sole claim on which to decide the appeal of the group.

With the aforementioned representation in mind, rather than reiterate the positions of the parties *in toto*, we focus on the issue therebetween. The Examiner finds, "[T]here does not appear to be support in the original disclosure for the claim limitation regarding the processor blocking colliding transactions." (Answer 3.) He further finds that "it is abundantly clear that the node controller is the element that directly performs the blocking *not* the processor." (*Id.* 11.) The Appellants allege, "Applicants' specification provides a written description that describes in detail the features of the claims." (Br. 5.) Therefore, the issue is whether the Appellants' original disclosure reasonably conveys to the artisan that they had possession of a processor that, after requesting a Read transaction, blocks transactions that collide with its transaction.

In addressing the issue, the Board conducts a two-step analysis. First, we construe the representative claim at issue to determine its scope. Second, we determine whether the construed claim had sufficient support.

#### A. CLAIM CONSTRUCTION

Our analysis begins with construing the claim limitations at issue. Claim 37 recites in pertinent part the following limitations: "abstaining, by said processor, from going critical by blocking transactions that collide with said Read transaction from being received by said processor during processing of said Read transaction. . . ." When the Appellants added these limitations to the claim, they interpreted the limitations to mean that "[t]he processor that requested the Read transaction then abstains from going critical by blocking transactions that collide with the Read transaction during the processing of the Read transaction." (Response to Office Action 6, filed Aug. 18, 2003.) Likewise, the Examiner interpreted these limitations to require that "the processor block[s] colliding transactions." (Answer 3.) In light of the interpretation shared by the Appellants and the Examiner, the limitations require a processor that, after requesting a Read transaction, blocks transactions that collide with its transaction.

#### B. WRITTEN DESCRIPTION DETERMINATION

"[C]ompliance with the 'written description' requirement of ' 112 is a question of fact. . . ." *Vas-Cath, Inc. v. Mahurkar*, 935 F.2d 1555, 1563, 19 USPQ2d 1111, 1116 (Fed. Cir. 1991) (citing *In re Gosteli*, 872 F.2d 1008, 1012, 10 USPQ2d 1614, 1618 (Fed. Cir. 1989); *Utter v. Hiraga*, 845 F.2d 993, 998, 6 USPQ2d 1709, 1714 (Fed. Cir. 1988)). "[T]he test for

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sufficiency of support . . . is whether the disclosure of the application relied upon 'reasonably conveys to the artisan that the inventor had possession at that time of the later claimed subject matter.'" *Ralston Purina Co. v. Far-Mar-Co., Inc.*, 772 F.2d 1570, 1575, 227 USPQ 177, 179 (Fed. Cir. 1985) (quoting *In re Kaslow*, 707 F.2d 1366, 1375, 217 USPQ 1089, 1096 (Fed. Cir. 1983)). "Application sufficiency under ' 112, first paragraph, must be judged as of the filing date [of the application]." *Vas-Cath*,, 935 F.2d at 1566, 19 USPQ2d at 1119 (citing *United States Steel Corp. v. Phillips Petroleum Co.*, 865 F.2d 1247, 1251, 9 USPQ2d 1461, 1464 (Fed. Cir. 1989)).

Here, we agree with the Examiner that "it is important to note that the claim language in question (the processor performing the blocking) was added by amendment on 8/18/03. . . ." (Answer 14.) In other words, the limitations that require a processor that, after requesting a Read transaction, blocks transactions that collide with its transaction were absent from the original claims.

Turning to the original disclosure, the Examiner has identified "**nineteen recitations of blocking by the node controller . . . not the processor.**" (Answer 11.) Among these recitations is the one cited by the Appellants in their aforementioned amendment, viz., "the specification at page 56, lines 13-21." (Response to Office Action 6, filed Aug. 18, 2003.) Like the other eighteen recitations, rather than describing a processor blocking colliding transactions, however, this recitation explains that "the

node controller selectively blocks colliding transactions. . . ." (Specification 56: 19-21.)

For their part, the Appellants now allege that three parts of the Specification support the added limitations. First, they allege that "support for Applicants' claims can be found in the specification on page 61, line 24, through page 62, line 19. Applicants describe a processor blocking its ordinary responses by providing modified responses instead." (Br. 5.) Although this part of the specification explains that "the processors in a distributed, multi-bus, multiprocessor system are required to abstain from going critical upon receiving a RemStat AResp signal for their own Reads," (Specification 61: 12-15), it does not mention "blocking," let alone blocking performed by the processors.

Second, the Appellants allege that according to "specification page 60, line 32, through page 61, line 2," (Br. 5), "if the processor has a copy of the cache line in a Shared state and has an outstanding Read transaction, the processor must produce a 'Shared AResp', not a 'Retry'. A 'Retry' is also blocked by the processor in this situation." (*Id.*) Although this part of the specification explains that "a colliding snooped Read transaction was blocked **from** a processor," (Specification 60: 26-27 (emphasis added)), it does not mention what element actually blocks the transaction from reaching the processor. Step 1318 of the Appellants' Figure 13, however, discloses that it is the "[n]ode controller [that] blocks snooped Read transactions from the processor. . . ."

Third, the Appellants note, "The specification also states that if the processors block the ordinary protocol responses, no external logic is needed to block colliding Read transactions. 'If the processors do implement the RemStat-related requirements, then the processors may run without inclusion, and no external logic is needed to detect the Read-Read collision and to block colliding Read transactions.' See specification page 63, lines 17-21." (Br. 5.) Although this part of the specification describes blocking, it does not disclose that the processors perform the blocking. To the contrary, the part teaches that the "blocking [is] implemented in the bridge chip, e.g., the node controllers in the distributed, multi-bus, multiprocessor system. . . ." (Specification 63: 14-16.)

For the aforementioned reasons, we agree with the Examiner's finding that the Appellants' original disclosure fails to reasonably convey to the artisan that they had possession, as of the filing date of their application, of a processor that, after requesting a Read transaction, blocks transactions that collide with its transaction. Therefore, we affirm the written description rejection of claim 37 and of claims 38-48 and 60-65, which fall therewith.

### III. ANTICIPATION AND OBVIOUSNESS REJECTIONS

The Examiner makes the following allegations.

Donaldson *et al.* disclose . . . abstaining by said processor from going critical by blocking transactions that collide with said Read transaction from being received by said processor during processing of said transaction, in response to receiving, by said processor, a coherency response indicating state information for data to be read by the Read transaction will be delivered along with delivery of the data, said processor and said other

processors being prohibited from gaining ownership of said cache line during said processing of said Read transaction, wherein Read-Read deadlocks are prohibited, by teaching in column 6, lines 42-51, a FORWARD-EXCLUSIVE state wherein the data block is present in exactly one cache memory and is modified.

(Answer 4.) The Appellants argue, "*Donaldson* does not describe blocking transactions that collide with the Read transaction from being received by the processor during processing of the Read transaction. *Donaldson* teaches stopping the processing of new read commands, not blocking transactions from being received." (Reply Br. 3.) They further argue that "the combination of *Donaldson* and *Arimilli* does not render Appellant's claims unpatentable because *Arimilli* does not cure the deficiencies of *Donaldson*." (Reply Br. 3.) Therefore, the issue is whether *Donaldson* blocks colliding transactions from being received by a processor that requested a Read transaction.

In addressing the issue, the Board conducts a two-step analysis. First, we construe independent claims at issue to determine their scope. Second, we determine whether the construed claims are anticipated.

#### A. CLAIM CONSTRUCTION

"The Patent and Trademark Office (PTO) must consider all claim limitations when determining patentability of an invention over the prior art." *In re Lowry*, 32 F.3d 1579, 1582, 32 USPQ2d 1031, 1034 (Fed. Cir. 1994) (citing *In re Gulack*, 703 F.2d 1381, 1385, 217 USPQ 401, 403-04 (Fed. Cir. 1983)).

Here, claims 37 and 60 recite in pertinent part the following limitations: "blocking transactions that collide with said Read transaction from being received by said processor during processing of said Read transaction. . . ." Considering these limitations, the independent claims require blocking colliding transactions from being received by a processor that requested a Read transaction.

#### B. ANTICIPATION DETERMINATION

"Having construed the claim limitations at issue, we now compare the claims to the prior art to determine if the prior art anticipates those claims." *In re Cruciferous Sprout Litig.*, 301 F.3d 1343, 1349, 64 USPQ2d 1202, 1206 (Fed. Cir. 2002). "[A]n invention is anticipated if the same device, including all the claim limitations, is shown in a single prior art reference. Every element of the claimed invention must be literally present, arranged as in the claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed.Cir. 1989) (citing *Perkin-Elmer Corp. v. Computervision Corp.*, 732 F.2d 888, 894, 221 USPQ 669, 673 (Fed. Cir. 1984); *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 771-72, 218 USPQ 781, 789 (Fed. Cir. 1983)). "[A]bsence from the reference of any claimed element negates anticipation." *Kloster Speedsteel AB v. Crucible, Inc.*, 793 F.2d 1565, 1571, 230 USPQ 81, 84 (Fed. Cir. 1986).

Here, Donaldson describes "[a] cache coherency protocol for a multi-processor system which provides for read/write, read-only and transitional data states and for an indication of these states to be stored in a memory

directory in main memory." (Abs. ll. 1-4.) "FIG. 1 is a block diagram of [the] multi-processor system. . . ." (Col. 4, ll. 65-66.) The Figure shows that "[e]ach one of several nodes, for example, four central processing units (CPU's) 10, 11, 12 and 13 includes a write back cache memory 30 . . . and is coupled by a channel 14, 15, 16 and 17, respectively, to a cross bar switch unit 18." (Col. 5, ll. 15-19.) "Moreover, each of several (for example, four) main memory modules 22, 23, 24, 25 is coupled by channels 26, 27, 28 and 29, respectively, to the cross bar switch unit." (*Id.* ll. 22-25.)

The part of Donaldson relied on by the Examiner describes a "FORWARD-EXCLUSIVE," (col. 6, l. 42), ownership state of a "data block residing in the main memory module 22-25." (*Id.* ll. 18-19.) In this state, explains the reference, "[a]ny additional read commands to this block force the main memory module 22-25 to stop processing all new read commands until the outstanding Read Exclusive is completed." (*Id.* ll. 46-49.) Based on this explanation, we agree with the Appellants that the FORWARD-EXCLUSIVE state "does not describe blocking transactions that collide with the Read transaction from being received by the processor during processing of the Read transaction." (Reply Br. 3.) This state merely stops the processing of new read commands.

The absence of blocking colliding transactions from being received by a processor that requested a Read transaction negates anticipation. Therefore, we reverse the anticipation rejection of claims 37 and 60 and of claims 38-40, 42-48, 61-63, and 65, which depend therefrom. The Examiner

does not allege, let alone show, that the addition of Arimilli cures the aforementioned deficiency of Donaldson. Therefore, we also reverse the obviousness rejection of claims 38-48 and 61-65.

#### IV. CONCLUSION

In summary, the rejection of claims 37-48 and 60-65 under 35 U.S.C. § 112, ¶ 1, is affirmed. The rejection of claims 37-40, 42-48, 60-63, and 65 under § 102(e) and the rejection of claims 38-48 and 61-65 under § 103(a), however, are reversed.

"Any arguments or authorities not included in the brief or a reply brief filed pursuant to [37 C.F.R.] § 41.41 will be refused consideration by the Board, unless good cause is shown." 37 C.F.R. § 41.37(c)(1)(vii). Accordingly, our affirmance is based only on the arguments made in the briefs. Any arguments or authorities omitted therefrom are neither before us nor at issue but are considered waived. *Cf. In re Watts*, 354 F.3d 1362, 1367, 69 USPQ2d 1453, 1457 (Fed. Cir. 2004) ("[I]t is important that the applicant challenging a decision not be permitted to raise arguments on appeal that were not presented to the Board.")

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No time for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

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