The opinion in support of the decision being entered today
was **not** written for publication and
is **not** binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte CHRISTOPHER L. HAMLIN

Appeal No. 2006-0167
Application No. 10/186,263

ON BRIEF

Before: HAIRSTON, DIXON and NAPPI, **Administrative Patent Judges**.

NAPPI, **Administrative Patent Judge**.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 of the final rejection of claims 1 through 11, 14 through 24 and 27.[1] For the reasons stated *infra* we affirm-in-part the examiner's rejection of these claims.

[1] We note that the examiner withdrew the rejection of claims 12 and 25. See page 3 of the examiner's answer.

Invention

The invention relates to a timing abstraction and portioning strategy for integrated circuit design. See page 1 of appellant's specification.

Claim 1 is representative of the invention and is reproduced below:

1. A method of designing an integrated circuit, comprising:

monitoring user interaction with logical blocks during a functional design process of an integrated circuit; and

deriving, without affecting the functional design process, indications of timing properties during the functional design process based on the monitored user interaction, the indications of timing properties including background heuristics describing timing properties of the logical blocks within a hierarchy of functional elements of the integrated circuit,

wherein the indications of timing properties are used during back end stages to complete timing closure and verification after completion of the functional design process.

Reference

The reference relied upon by the examiner is:

Chang et al. (Chang)	6,594,800	July 15, 2003 (filed Jan. 4, 2001)

Opinion

We have carefully considered the subject matter on appeal, the rejection advanced by the examiner and the evidence of anticipation relied upon by the examiner as support for the rejection. We have, likewise, reviewed and taken into consideration, in reaching our decision, appellant's arguments set forth in the

briefs along with the examiner's rationale in support of the rejection and arguments in rebuttal set forth in the examiner's answer.

With full consideration being given to the subject matter on appeal, the examiner's rejection and the arguments of appellant and the examiner, and for the reasons stated *infra* we sustain the examiner's rejections of claims 1 through 10, 14 through 23 and 27under 35 U.S.C. § 102(e). However, we will not sustain the examiner's rejections of claims 11 and 24 under 35 U.S.C. § 102(e).

Grouping of the claims.

At the outset, we note that appellant's arguments group the claims in two (2) groups. On pages 4 and 5 of the brief appellant provides arguments directed to claims 1 through 10, 14 through 23 and 27. On page 6 of the brief, appellant provides arguments as to why the limitations common to claims 11 and 24 are not taught by Chang. Accordingly, we will address these claims as grouped by appellant's arguments.

Rejection of claims 1 through 10, 14 through 23 and 27

under 35 U.S.C. § 102(e).

Appellant argues, on page 5 of the brief, that the examiner has not addressed the limitation "without affecting the functional design process" in rejecting the claims. Further, appellant argues:

> [I]n rejecting independent Claims 1, 14 and 27, the Examiner alleged that "the timing model (timing properties of the logical blocks) is obtained from Front-end acceptance stage (102) as <u>a result of monitoring</u> user interaction with logical blocks corresponding to a hierarchy of functional elements (col. 2, ll. 35-36, col. 10, ll. 44-46)" (emphasis added) (Office Action 12/22/2004, page 3, lines 3-6). Applicant respectfully submits that this allegation is *not* even supported by the Examiner's own citation.

Appellant additionally argues, on page 6 of the reply brief:

> However, even though the front-end acceptance stage feeds information to a timing model according to Chang, nowhere in Chang was it taught, disclosed or suggested that the timing model is obtained <u>as a result of</u> monitoring user interaction with logic blocks. As is well known by those of ordinary skill in the art, there are many steps included in the front-end design state. However, the front-end design stage may *or* may not include a step of monitoring user interaction with logic blocks. Thus, the fact that the front-end acceptance stage feeds information to a timing model does *not* mean that the timing model is obtained as a result of monitoring user interaction with logic blocks, since the front-end acceptance stage may *not* include the step of monitoring user interaction with logic block, *and/or* the timing model may be obtained as a result of steps included in the front-end acceptance stage other than the step of monitoring user interaction with logic blocks.

The examiner states on page 5 of the answer:

> Chang et al. discloses a method of designing an integrated circuit using a design process based on the **block-based design** (BBD) methodology including front-end acceptance design stage, such as **selecting the logical blocks** for design and **collecting the estimation data** for each block (column 8, lines 21-27), using a **Scan Design methodology** (monitoring) (column 4, lines 2, 3) "without affecting the functional design process" as shown on the Figure 1, wherein during the design process, front-end acceptance **design stage**, not only performs their intended functions, but also generate the information needed for **timing verification** (column 9, lines 66, 67; column 10, lines 1-4).

Further, the examiner states on pages 5 and 6 of the answer that the limitation:

"without affecting functional design process" was not ignored, but rather considered as a negative limitation and that Chang does not teach that deriving the timing properties affects the functional design process.

Additionally, the examiner states on pages 6 and 7 of the answer:

> Chang et al., column 9, lines 43-45 discloses that **timing margin specification** (containing information for each circuit block) is received from the front-end acceptance design stage as observed from Figure 8, wherein the block named "Create Timing Environment" is fed by the information coming from front-end acceptance design stage (column 10, lines 44-46). Furthermore Chang et al. discloses that **timing verification** can be performed during front-end acceptance design stage (column 9, lines 60-63), which means that **timing verification** is produced based on the information obtained by the front-end acceptance design stage.

We concur with the examiner. Claim 1 includes the limitation "deriving, without affecting the functional design process, indications of timing properties during the functional design process based on the monitored user interaction." We find no disclosure in Chang that suggests that the derivation of timing indications affect the functional design process. Thus, we are not persuaded by appellant's arguments that the examiner ignored these limitations.

Similarly, we are not persuaded by appellant's argument that Chang does not teach that the timing is obtained from the front-end acceptance stage. Appellant's argument is not commensurate with the scope of the claim. Claim 1 includes the limitation of deriving "indications of timing properties during the functional design process" and "the indications of timing properties are used during back end stages to compete timing closure and verification after completion of the functional design process." In analyzing the scope of the claim,

office personnel must rely on appellant's disclosure to properly determine the meaning of the terms used in the claims. ***Markman v. Westview Instruments, Inc.***, 52 F3d 967, 980, 34 USPQ2d 1321, 1330 (Fed. Cir. 1995). "[I]nterpreting what is *meant* by a word in a claim 'is not to be confused with adding an extraneous limitation appearing in the specification, which is improper.'" (emphasis original) ***In re Cruciferous Sprout Litigation,*** 301 F.3d 1343, 1348, 64 USPQ2d 1202, 1205, (Fed. Cir. 2002) (citing ***Intervet America Inc v. Kee-Vet Laboratories Inc.,*** 887 F.2d 1050, 1053, 12 USPQ2d 1474, 1476 (Fed. Cir. 1989). Thus, we do not find that claim 1 requires obtaining the timing model as a result of monitoring, but rather that indications of the timing are derived as a result of monitoring user interaction. Appellant's specification identifies that these indication may be "hints" and may include "likely timing properties of logical blocks." Thus, we do not consider "indications of timing properties" to be synonymous with "timing model".

We find, as the examiner asserts, Chang teaches a block based design methodology for integrated circuits. Further, we find that Chang, in Figure 1, and column 9, lines 55 through 65, teaches that timing verification can be performed at each stage of design, thus implying that timing information is derived at each stage of design. Accordingly, we are not persuaded by appellant's arguments that the examiner has not set forth a ***prima facie*** case of anticipation and, we sustain the examiner's rejection of claims 1 through 10, 14 through 23 and 27 under 35 U.S.C. § 102(e).

Rejection of claims 11 and 24 under 35 U.S.C. § 102(e).

Appellant argues on page 6 of the brief:

> Chang's absolute constraints, relative constraints, and mixed constraints fail to teach, disclose or suggest "the mathematical formulation including functional description of the integrated circuit, block structure in which a relationship of logical blocks is expressed, hierarchy in which the logical blocks are expressed' (emphasis added), as recited in Claims 11 and 24.

In response the examiner asserts, on page 7 of the answer, that Chang in column 17 describes a mathematical formulation between the expected value of the design and design decision constraint. On page 8 of the answer, the examiner asserts that the absolute block constraints include timing indications and are mathematically described in formulas discussed in column 17. Further, the examiner states that column 43 identifies that the blocks are expressed hieratically. Thus, the examiner concludes that Chang teaches the limitations of claims 11 and 24.

We disagree with the examiner's rationale. Claims 11 and 24 include the limitation of "the mathematical formulation including functional description of the integrated circuit, block structure in which a relationship of logical blocks is expressed, hierarchy in which the logical blocks are expressed, timing implications of logical blocks in terms of timing specification for the integrated circuit, content of timing indications and structure of timing indications." Thus, claims 11 and 24 require the mathematical formulation to include six things, including the relationship of logical blocks and hierarchy in which the logical

blocks are expressed. We find that Chang's equations in column 17, lines 17 through 21, which the examiner relies upon to support the rejection, do not teach the relationship between blocks nor the hierarchy of blocks. Chang teaches that the formula $BDC_{block}=A.C_{block._block}$ represents the design constraint for a block and does not indicate the interconnection between blocks nor the hierarchy of blocks. See column 17, line 17. Thus, we do not find that Chang teaches all of the limitations of claims 11 and 24. Accordingly, we will not sustain the examiner's rejection of claims 11 and 24.

Summary

Only those arguments actually made by appellant have been considered in this decision. Arguments which appellant could have made but chose not to make in the brief or by filing a reply brief have not been considered and are deemed waived by appellant (see 37 CFR § 41.37(c)(vii)). Support for this rule has been demonstrated by our reviewing court in ***In re Berger***, 279 F.3d 975, 984, 61 USPQ2d 1523, 1528-1529 (Fed. Cir. 2002) wherein the Federal Circuit stated that because the appellant did not contest the merits of the rejections in his brief to the Federal Circuit, the issue is waived***. See also In re Watts***, 354 F.3d 1362, 1368, 69 USPQ2d 1453, 1458 (Fed. Cir. 2004).

In summary, we sustain the examiner's rejection of claims 1 through 10, 14 through 23 and 27under 35 U.S.C. § 102(e). However, we will not sustain the examiner's rejection of claims 11 and 24 under 35 U.S.C. § 102(e). The decision of the examiner is affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR §1.136(a)(1)(iv).

AFFIRMED-IN-PART

KENNETH W. HAIRSTON Administrative Patent Judge	)	
JOSEPH L. DIXON Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
ROBERT E. NAPPI Administrative Patent Judge	)	

REN/gjh

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