

The opinion in support of the decision being entered today was not written for publication and is *not* binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte VADIM V. IVANOV, SHOUBAO YAN and WALTER B. MEINEL

Appeal No. 2006-0380
Application 10/445,783

ON BRIEF

Before THOMAS, BARRETT and OWENS, *Administrative Patent Judges*.
OWENS, *Administrative Patent Judge*.

DECISION ON APPEAL

This appeal is from a rejection of claims 1-3 and 15-17.
Claims 4-14, 18 and 19 have been canceled, and claims 20-24 have
been withdrawn from consideration.

THE INVENTION

The appellants claim a CMOS circuit having feedback circuits that prevent pull-up and pull-down transistors from being on simultaneously. Claim 1 is illustrative:

1. A CMOS circuit including a pull-up transistor and a pull-down transistor, comprising:

(a) a first feedback circuit having an input directly coupled to a gate of the pull-up transistor and an output coupled to a gate of the pull-down transistor;

(b) a second feedback circuit having an input directly coupled to the gate of the pull-down transistor and an output coupled to the gate of the pull-up transistor;

(c) the first feedback circuit producing a first delayed signal on the gate of the pull-down transistor to turn on the pull-down transistor a first predetermined amount of time after the pull-up transistor is turned completely off so as to prevent any shoot-through current from flowing through the pull-up transistor and the pull-down transistor; and

(d) the second feedback circuit producing a second delayed signal on the gate of the pull-up transistor to turn on the pull-up transistor a second predetermined amount of time after the pull-down transistor is turned completely off so as to prevent any shoot-through current from flowing through the pull-up transistor and the pull-down transistor.

THE REFERENCES

McClure	5,349,243	Sep. 20, 1994
Nolan	6,653,878	Nov. 25, 2003
		(filed Sep. 24, 2001)

THE REJECTIONS

The claims stand rejected as follows: claims 1, 3 and 15-17 under 35 U.S.C. § 102(b) as being anticipated by McClure, and claims 1-3 and 15-17 under 35 U.S.C. § 102(e) as being anticipated by Nolan.

OPINION

We affirm the aforementioned rejections.

Rejection over McClure

McClure discloses a latch controlled output driver (90) comprising 1) latches 94 and 96, each having a PMOS transistor (P1 and P2, respectively), and 2) an output driver (92) comprising NMOS pull-up (T1) and pull-down (T2) transistors (col. 2, line 48 - col. 3, line 3). Latches 94 and 96 are connected, respectively, to the gates of transistors T1 and T2 (abstract; figure 2). Transistors P1 and P2 ensure that transistors T1 and T2 are not on at the same time (col. 1, line 68 - col. 2, line 4; col. 3, lines 36-41).

The appellants argue that in McClure “[t]here is no mention of a delay signal” (brief, page 10).

Like the appellants' pull-up and pull-down transistors, there necessarily is a delay when McClure's pull-up and pull-down transistors turn off. Because McClure's feedback circuit (figure 2), like that of the appellants (figure 1), prevents the pull-up and pull-down transistors from being on at the same time, then like the appellants' feedback circuit, McClure's feedback circuit necessarily provides a delay signal.

We therefore are not convinced of reversible error in the examiner's rejection of the appellants' claims over McClure. Accordingly, we affirm the rejection over that reference.

Rejection over Nolan

Nolan discloses a comparator output controlled circuit comprising 1) a break before make circuit (104) having a NAND gate (216), a NOR gate (226) and inverters (218, 220, 222, 228, 230 and 232), 2) a slew rate control circuit (106) having two capacitors (236 and 238) and a resistor (239),¹ and 3) an output buffer (108) having a PMOS driver (240) and an NMOS driver (241)

¹ "The slew rate is approximately equal to the current from either the NAND gate **216** or NOR gate **226** divided by the capacitance **236** or **238** respectively" (col. 5, lines 7-9).

(col. 4, lines 13-50). The make before break circuit provides non-overlap delay between the time when the PMOS driver turns off and the NMOS driver turns on, and vice versa (col. 4, lines 51-58; col. 5, lines 43-65).

The appellants argue that inverters 218 and 228 are connected to slew rate control circuit 106 and, therefore, are not directly connected, respectively, to transistors 240 and 241 (brief, page 11).

Nolan's inverters 218 and 228 are connected in parallel with, respectively, capacitors 236 and 238 of the slew rate circuit and transistors 240 and 241 of the output buffer (figure 2). Inverters 218 and 228, therefore, are directly connected to both capacitors 236 and 238, respectively, and transistors 240 and 241, respectively.

Accordingly, we affirm the rejection over Nolan.

DECISION

The rejections of claims 1, 3 and 15-17 under 35 U.S.C. § 102(b) over McClure, and of claims 1-3 and 15-17 under 35 U.S.C. § 102(e) over Nolan, are affirmed.

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No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a)(1)(iv).

AFFIRMED

JAMES D. THOMAS)
Administrative Patent Judge)
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) BOARD OF PATENT
LEE E. BARRETT)
Administrative Patent Judge) APPEALS AND
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) INTERFERENCES
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