

The opinion in support of the decision being entered today was *not* written for publication and is *not* binding precedent of the Board.

**UNITED STATES PATENT AND TRADEMARK OFFICE**

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**BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES**

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Ex parte PHILIP B. JAMES-ROXBY, DANIEL J. DOWNS,  
RUSSELL J. MORGAN, and CAMERON D. PATTERSON

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Appeal No. 2006-1184  
Application No. 10/102,585

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ON BRIEF

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Before KRASS, JERRY SMITH, and BARRY, Administrative Patent Judges.

JERRY SMITH, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134 from the examiner's rejection of claims 1-3, 7, and 14. Claim 4 has been indicated to contain allowable subject matter.

The disclosed invention pertains to implementing a circuit on a programmable logic device (PLD) that integrates a high-level static circuit design with a run-time parameterizable (RTP) logic core. Specifically, the invention generates a configuration bitstream from a main circuit design that is specified in a hardware description language (HDL). The main circuit design includes a first sub-circuit design that specifies a selected subset of resources of the PLD needed by the RTP core and an interface between the RTP core and other parts of the main circuit design. In the configuration bitstream, the configuration data corresponding to the first sub-circuit design are replaced with configuration data that implement the RTP core via executing a run-time reconfiguration control program. The run-time reconfiguration program then configures the PLD with the updated configuration bitstream.

Representative claim 1 is reproduced as follows:

1. A computer-implemented method for implementing a circuit on a programmable logic device (PLD), from a circuit design defined by a high-level static circuit design and a run-time parameterizable (RTP) core, comprising:

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generating a configuration bitstream from a main circuit design specified in a hardware description language and including a first sub-circuit design that specifies a selected subset of resources of the PLD needed by the RTP core and an interface between the RTP core and other parts of the main circuit design;

replacing in the configuration bitstream configuration data that correspond to the first sub-circuit design with configuration data that implement the RTP core, via execution of a run-time reconfiguration control program; and

configuring the PLD with the configuration bitstream after replacement of the selected data under control of the run-time reconfiguration control program.

The examiner relies on the following references:

Blodget 6,510,546 Jan. 21, 2003  
(filed Jul. 13, 2000)

Hyde, Daniel C., "CSCI 320 Computer Architecture Handbook on Verilog HDL," Computer Science Dept., Bucknell Univ., Aug. 1995 (Updated Aug. 1997).

IEEE Dictionary, 7th ed. (date unknown).

The following rejection is on appeal before us:

Claims 1-3, 7, and 14 stand rejected under 35 U.S.C.

§ 102(e) as being anticipated by Blodget.

Rather than repeat the arguments of appellants or the examiner, we make reference to the briefs and the answer for the respective details thereof.

OPINION

We have carefully considered the subject matter on appeal, the rejection advanced by the examiner and the evidence of anticipation relied upon by the examiner as support for the rejection. We have, likewise, reviewed and taken into consideration, in reaching our decision, appellants' arguments set forth in the briefs along with the examiner's rationale in support of the rejection and arguments in rebuttal set forth in the examiner's answer.

It is our view, after consideration of the record before us, that the disclosure of Blodget does not fully meet the invention as set forth in claims 1-3, 7, and 14. Accordingly, we reverse.

Anticipation is established only when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of a claimed invention as well as disclosing structure which is capable of performing the recited functional limitations. RCA Corp. v. Applied Digital Data Systems, Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir.); cert. dismissed, 468 U.S. 1228 (1984); W.L. Gore and Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 1554, 220 USPQ 303, 313 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984).

The examiner has indicated how the claimed invention is deemed to be fully met by the disclosure of Blodget [answer, pages 4 and 5; final rejection, pages 2-4]. Appellants argue that Blodget does not teach that the hardware description language (HDL) specification includes a sub-circuit design that specifies programmable logic device (PLD) resources needed by the run-time parameterizable (RTP) core. Appellants further argue that Blodgett does not teach replacing, in the configuration bitstream, configuration data corresponding to these resources with configuration data that implements the RTP core [brief, page 5]. Specifically, appellants note that the cores in Blodget are implemented as Java classes, but skilled artisans would not recognize Java as an HDL as claimed [brief, page 5; reply brief, pages 2 and 3].

Appellants note that although Blodget discloses generating a configuration bitstream from an HDL design in Fig. 1, HDL is not used in Blodget's run-time reconfiguration flow. Appellants argue that Blodget actually contrasts static design flow (i.e., utilizing HDL) in Fig. 1 from run-time reconfiguration design flow in Fig. 2 [brief, page 4].

The examiner quotes an excerpt from a handbook on Verilog HDL that "HDL is a language used to describe a layout of the wires, resistors, transistors, logical gates and flip flops on an Integrated Circuit (IC) chip" [answer, page 6]. Using this construction, the examiner argues that Blodget's code listing shown on col. 9, line 38 - col. 10, line 3 (specifying component pin locations and routing between the pins) constitutes HDL that is used as input data for pre-routing tool 252. The examiner further argues that the bit-level interface code generated by pre-routing tool 252 constitutes a bitstream and that edit process 256 replaces or edits the configuration bitstream upon execution of the run-time reconfiguration program code [answer, pages 7 and 8].

Appellants contend that the examiner's construction of HDL as claimed is unreasonably broad since, under the examiner's definition, the skilled artisan would be unable to distinguish an HDL from a non-HDL [reply brief, page 3]. Appellants further note that not only does the handbook cited by the examiner not reference a high-level programming language such as Java as being

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an HDL, the reference actually identifies Verilog and VHDL as the two main HDLs -- the same two HDLs identified on Page 1 of the present application as exemplary [reply brief, page 3].

We will not sustain the examiner's rejection. We agree with appellants that Blodget does not reasonably teach or suggest specifying a main circuit design specified in an HDL in the preferred embodiment, let alone generating a configuration bitstream from the HDL's main circuit design and replacing configuration data in the configuration bitstream with configuration data implementing the RTP core via execution of a run-time reconfiguration control program as claimed. In short, on the record before us, Blodgett's use of Java in the preferred embodiment is not an HDL as recognized by skilled artisans.

Although Blodget discloses generating a configuration bitstream from an HDL-based design in connection with the admitted prior art circuit design approach in Fig. 1 and col. 3, lines 13-49, Blodget's teachings actually run counter to HDL design approaches in run-time reconfigurable systems such as the

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Java-based system disclosed in the preferred embodiment. Indeed, Blodget states that not only does the prior art HDL-based approach provide "no support for run-time reconfiguration[,]...it is difficult to imagine constructs to support run-time reconfiguration in environments based on schematic or HDL design entry" [Blodget, col. 3, lines 44-49].

Furthermore, the handbook excerpt cited by the examiner expressly states that hardware designers in industry and academia use two major HDLs -- Verilog and VHDL [Handbook, Section 1.1, ¶ 1]. See also id., Section 1.3, ¶ 1 ("The most prominent modern HDLs in industry are Verilog and VHDL."). According to the article, "Verilog HDL allows a hardware designer to describe designs at a high level of abstraction such as at the architectural or behavioral level as well as the lower implementation levels (i.e., gate and switch levels) leading to Very Large Scale Integration (VLSI) Integrated Circuits (IC) layouts and chip fabrication" [id., Section 1.1, ¶ 3]. Notably, high-level programming languages such as Java are not mentioned as HDLs.

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During patent examination, the pending claims must be "given their broadest reasonable interpretation consistent with the specification." In re Hyatt, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000). But the broadest reasonable interpretation of the claims must also be consistent with the interpretation that those skilled in the art would reach. In re Cortright, 165 F.3d 1353, 1358, 49 USPQ2d 1464, 1467 (Fed. Cir. 1999). See also MPEP § 2111. Thus, claim terms must be given their plain meaning unless applicant has provided a clear definition in the specification. In re Zletz, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989). See also MPEP § 2111.01(I). The "plain meaning" of a claim term refers to its ordinary and customary meaning -- the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention. See Phillips v. AWH Corp., 415 F.3d 1303, 1312-13, 75 USPQ2d 1321, 1326-27 (Fed. Cir. 2005) (en banc). "The person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification" [id.]. See also MPEP § 2111.01(II).

Based on the record before us and in light of the specification, we conclude that the skilled artisan would reasonably interpret HDL as claimed as a unique specialized circuit design language such as Verilog or VHDL -- not a high-level programming language such as Java. As noted previously, the context of Blodget favors our interpretation and the handbook excerpt supplied by the examiner mentions only Verilog and VHDL as major HDLs. We therefore conclude that the broadest reasonable interpretation of a main circuit design specified in HDL would not reasonably include Blodget's preferred embodiment utilizing Java. Consequently, Blodget does not disclose, teach, or suggest generating a configuration bitstream from a main circuit design specified in an HDL as claimed in the independent claims, let alone replacing configuration data in the configuration bitstream with configuration data implementing the RTP core via execution of a run-time reconfiguration control program. Since we do not sustain the examiner's rejection of independent claims 1 and 14, we likewise do not sustain the examiner's rejection of dependent claims 2, 3, and 7.

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In summary, we have not sustained the examiner's rejection with respect to any of the claims on appeal. Therefore, the decision of the examiner rejecting claims 1-3, 7, and 14 is reversed.

REVERSED

ERROL A. KRASS	)
Administrative Patent Judge	)
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	)
JERRY SMITH	) BOARD OF PATENT
Administrative Patent Judge	) APPEALS AND
	) INTERFERENCES
	)
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LANCE LEONARD BARRY	)
Administrative Patent Judge	)

JS/ce

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XILINX, INC  
ATTN: LEGAL DEPARTMENT  
2100 LOGIC DR  
SAN JOSE CA 95124