

The opinion in support of the decision being entered today was *not* written for publication and is *not* binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte FENG LIN and BRIAN JOHNSON

Appeal No. 2006-1204
Application No. 10/379,006

ON BRIEF

Before HAIRSTON, KRASS, and HOMERE, **Administrative Patent Judges.**

HOMERE, **Administrative Patent Judge.**

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1, 2, 5, 9-11, 13, 14, 22, 24, 25, 40, 45, 50, and 55. The Examiner has objected¹ to claims 3, 4, 6-8, 12, 15-21, 23, 26, 41-44, 46-49, 51-54, and 56-59. Claims 37-39 have been allowed.

¹ We note that claims 3, 4, 6-8, 12, 15-21, 23, 26, 41-44, 46-49, 51-54 and 56-59 were objected to in the final office action as being dependent upon a rejected base claim, and that none of the cited claims was actually rejected.

We also note that Appellants' proposed amendment rewriting the cited claims in independent form to include the limitations of the base claims and any intervening claims was not entered. Additionally, we note that the cited claims as presented on appeal are "objected to". We have consequently declined to rule on the merits of the Examiner's objection to the cited claims or the Examiner's refusal to enter the proposed amendment since such issues are not properly appealable before the Board of Patent Appeals and Interferences. See 35 U.S.C. § 134.

Invention

Appellants' invention relates generally to a method, an apparatus, and a computer-readable storage medium containing instructions for calibrating the impedance of a driver circuit (225) in an integrated circuit (IC) package (200), as depicted in figure 2. The driver circuit (225) has a plurality of impedances (300) and is coupled to an external load (210) through a PAD (215), which provides a path (220) for signals to pass from the driver circuit and the load. See also figure 3A. The IC package (200) includes a synchronous circuit (260) that monitors the phase difference between one or more internal clock signals and an external clock signal. See also figure 4, item 400. Upon detecting a phase difference between the clock signals, the synchronous circuit (260) issues an update signal (270) to a controller (230) indicative of a possible impedance mismatch between the driver circuit (225) and the external load (210). The controller (230) in turn sends a test signal (250) to a test driver circuit (240) and a resistor (245) to determine whether an

impedance mismatch actually exists between the external load (210) and the driver circuit (225). See also figure 4, item 410. In response, the test driver circuit (240) provides a signal

(255) confirming whether or not an actual impedance mismatch does exist. See also figure 4, item 420. Upon a determination that no impedance mismatch exists, no calibration is done. See also figure 4, item 430. In the event that an impedance mismatch is found to exist, the controller (230) issues a command to an arbiter (235) to select a new impedance for the driver circuit (225). See also figure 4, item 440. Depending on the state of the driver circuit (225), the arbiter (235) decides to either transmit the command to the driver circuit (225) or to return the command to the controller (230) for storage in the register (255). See also figure 4, items 450, 460, 470 and 480.

Claim 13 is representative of the claimed invention and is reproduced as follows:

13. An apparatus, comprising:

a driver circuit having a first plurality of impedances;

a load coupled to the driver circuit;

a synchronous circuit capable of providing a signal indicative of an impedance mismatch between the driver circuit and the load; and

a controller for selecting one of the first plurality of impedances to reduce the impedance mismatch in response to the signal.

Appeal No. 2006-1204
Application No. 10/379,006

References

The Examiner relies on the following reference:

Mooney et al. 6,087,847 July 11, 2000

Rejections At Issue

A. Claims 1, 2, 5, 9-11, 13, 14, 22, 24, 25, 50 and 55 stand rejected under 35 U.S.C. § 102 as being anticipated by Mooney et al.

B. Claims 40 and 45 stand rejected under 35 U.S.C. § 103 as being unpatentable over Mooney et al.

Rather than reiterating the arguments of Appellants and the Examiner, the opinion refers to respective details in the Brief² and the Examiner's Answer³. Only those arguments actually made by Appellants have been considered in this decision. Arguments, which Appellants could have made but chose not to make in the Brief have not been taken into consideration. See 37 CFR § 41.37(c)(1)(vii) (eff. Sept. 13, 2004).

OPINION

In reaching our decision in this appeal, we have carefully considered the subject matter on appeal, the Examiner's rejections, the arguments in support of the rejections and the evidence of anticipation and obviousness relied upon by the Examiner as support for the rejections. We have likewise

² Appellants filed an Appeal Brief on June 06, 2005.

³ The Examiner mailed an Examiner's Answer on August 26, 2005.

Appeal No. 2006-1204
Application No. 10/379,006

reviewed and taken into consideration Appellants' arguments set forth in the Brief along with the Examiner's rationale in support of the rejections and arguments in the rebuttal set forth in the Examiner's Answer. After full consideration of the record before us, we agree with Appellants that claims 1, 2, 5, 9-11, 13, 14, 22, 24, 25, 50 and 55 are not properly rejected under 35 U.S.C. § 102 as being anticipated by Mooney et al. We further agree with Appellants that claims 40 and 45 are not properly rejected under 35 U.S.C. § 103 as being unpatentable over Mooney et al. Accordingly, we reverse the Examiner's rejections of claims 1, 2, 5, 9-11, 13, 14, 22, 24, 25, 40, 45, 50 and 55 for the reasons set forth **infra**.

I. Under 35 U.S.C. § 102(b), is the Rejection of Claims 1, 2, 5, 9-11, 13, 14, 22, 24, 25, 50 and 55 as Being Anticipated By Mooney et al. Proper?

It is axiomatic that anticipation of a claim under § 102 can be found only if the prior art reference discloses every element of the claim. **See In re King**, 801 F.2d 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1986) and **Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.**, 730 F.2d 1452, 1458, 221 USPQ 481,

485 (Fed. Cir. 1984).

With respect to the Mooney et al. reference ("Mooney" hereinafter), Appellants argue that Mooney does not disclose a synchronous circuit as defined in the present application, nor does it teach the selection of an impedance from the driver circuit. In particular, at page 8 of the Brief, Appellants state that:

Mooney does not describe or suggest a synchronous circuit, as defined in the present application. Accordingly, Mooney fails to describe or suggest providing a signal from a synchronous circuit that is indicative of an impedance mismatch between a driver circuit and a load, as set forth in independent claims 1 and 13. Mooney also fails to describe or suggest selecting one of a plurality of impedances of the driver circuit to reduce the impedance mismatch in response to the signal, as set forth in independent

claims 1 and 13. Furthermore, Mooney fails to teach or suggest detecting an update signal from a synchronous circuit or modifying an impedance of the driver circuit in response to detecting the signal, as set forth in independent claims 50 and 55.

To determine whether claim 13 is anticipated, we must first determine the scope of the claim. We note that claim 13 reads in part as follows:

a synchronous circuit capable of providing a signal indicative of an impedance mismatch between the driver circuit and the load; and a controller for selecting one of the first plurality of impedances to reduce the impedance mismatch in response to the signal.

At page 15, lines 5-16, Appellants' specification states:

The package 200 typically includes the synchronous circuit 260 to synchronize one or more internal clock signals to an external clock signal. The internal clock signals may, in various alternative embodiments, be clock signals used by the internal circuitry 205, the arbiters 235, the driver circuits 225, and any other desirable circuitry in the package 200. For example, the synchronous circuit 260 may provide a synchronized clock signal 265 to the internal circuit 205. Examples of the synchronous circuit 260 include, but are not limited to delay-locked loops, phase-locked loops, and synchronous mirror delays. The synchronous circuit 260 monitors a phase difference between the one or more internal clock signals and the external clock signal and provides one or more adjustment signals in response to detecting the phase difference. In one embodiment, the synchronous circuit 260 may provide a fine adjustment signal in response to detecting small phase differences and a coarse adjustment signal in response to detecting large phase differences.

Further, at page 16, lines 5-17, Appellants' specification states:

Referring now to Figure 4, a flow chart illustrating one embodiment of a process of calibrating the driver circuits 225 is shown. In the illustrated process, a phase difference that may be indicative of an impedance mismatch is detected (at 400) by a synchronous circuit 260, which provides (at 410) the update signal 270 to the controller 230 in response to detecting (at 400) the phase difference. In response to the update signal 270, the controller 230 determines (at 420) whether an impedance mismatch may be present. If the controller 230 determines (at 420) that no mismatch is present, or that the impedance mismatch is small enough that it is not desirable to change the impedance of the driver circuit 225, the process ends (at 430). If the controller 230 determines (at 420) that the impedance mismatch is greater than a predetermined range of tolerance values, a determination may be made that it is desirable to change the impedance of the driver circuit 225 to reduce the impedance mismatch. The controller 230 then selects (at 440) one or more new impedances for the driver circuits 225.

Appeal No. 2006-1204
Application No. 10/379,006

Thus, the claim does require a synchronous circuit, and the selection of an impedance from the driver circuit.

Our reviewing court states in **In re Zletz**, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989) that "claims must be interpreted as broadly as their terms reasonably allow." Our reviewing court further states, "the 'ordinary meaning' of a claim term is its meaning to the ordinary artisan after reading the entire patent." **Phillips v. AWH Corp.**, 415 F.3d 1303, 1321, 75 USPQ2d 1321, 1332 (Fed. Cir. 2005).

Upon our review of Appellants' specification, we find that a discussion of the "synchronous circuit" was provided at page 15, lines 5-16, as reproduced above. Particularly, the cited portion of Appellants' specification indicates that the synchronous circuit serves the function of monitoring the phase difference between one or more internal clock signals and external clock signal to thereby synchronize the clock signals. We find that the ordinary meaning of the terms "synchronous circuit" is its meaning to the ordinary artisan after having read Appellants' entire specification. Consequently, the ordinarily skilled artisan would find the term "synchronous circuit" to mean a circuit capable of synchronizing signals of internal and external

clocks.

Now the question before us is what Mooney would have taught to one of ordinary skill in the art? To answer this question, we find the following facts:

1. Mooney states at column 5, lines 4-25 that:

As illustrated, an externally derived clock signal drives the control circuit; however, it is divided down by divider 442. Output buffer 320 comprises an interface circuit output buffer, while output buffer 330 comprises a non-data signal or "dummy" output buffer. A feedback control loop including amplifier

360 and impedance control logic 310 is coupled to adjust the impedance of output buffer 330 based, at least in part, on the impedance of external coupling 340. The feedback control circuit operates to approximately match the impedance of buffer 330 with, in this particular embodiment, the impedance of external resistor 340. Likewise, in this embodiment, resistors 370 and 350 effectively establish the voltage signal reference level for amplifier 360. Impedance control logic 310 based, at least in part, on the output signal of amplifier 360 controls whether to adjust the impedance of buffer 330 up or down, that is increase or decrease the buffer impedance. Likewise, this control signal information is also applied to buffer 320. The feedback control circuit also produces control signals to adjust the slew rate of buffer 320 based on the impedance control signals produced from operation of the feedback loop including buffer 330.

With the above discussion in mind, we find that Mooney teaches an externally derived clock signal that drives an

Appeal No. 2006-1204
Application No. 10/379,006

impedance control circuit (310), which is part of a feedback control loop that also includes a buffer (330) and an amplifier (360). We also find that Mooney teaches that the impedance control circuit (310) uses the output signal of the amplifier (360) to determine whether to increase or decrease the impedance of the buffer (330) to match it with the impedance of the external load (340), as well as to control the slew rate of

another buffer (320). One of ordinary skill in the art would have duly recognized that Mooney's teaching of only one external clock signal to drive the impedance control circuit does not amount to synchronizing signals of the internal and external clocks.

Further, the ordinarily skilled artisan would have duly recognized that Mooney's teaching of increasing or decreasing the impedance of the buffer does not amount to the claimed limitation of selecting one of the plurality of impedances from the circuit driver. Consequently, we find error in the Examiner's stated position, which concludes that Mooney teaches the claimed limitation of a synchronous circuit capable of providing a signal indicative of an impedance mismatch between the driver circuit

Appeal No. 2006-1204
Application No. 10/379,006

and the load; and a controller for selecting one of the plurality of impedances to reduce the impedance mismatch in response to the signal.

Therefore, we will not sustain the Examiner's rejection of claims 1, 2, 5, 9-11, 13, 14, 22, 24, 25, 50 and 55 under 35 U.S.C. § 102(b) as being anticipated by Mooney.

II. Under 35 U.S.C. § 103, is the Rejection of Claims 40 and 45 as Being Unpatentable over Mooney Proper?

In rejecting claims under 35 U.S.C. § 103, the Examiner bears the initial burden of establishing a **prima facie** case of obviousness. **In re Oetiker**, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). **See also In re Piasecki**, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984). The Examiner can satisfy this burden by showing that some objective teaching in the prior art or knowledge generally available to one of ordinary skill in the art suggests the claimed subject matter. **In re Fine**, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). Only if this initial burden is met does the burden of coming

Appeal No. 2006-1204
Application No. 10/379,006

forward with evidence or argument shift to the Appellants.

Oetiker, 977 F.2d at 1445, 24 USPQ2d at 1444. **See also Piasecki**, 745 F.2d at 1472, 223 USPQ at 788.

An obviousness analysis commences with a review and consideration of all the pertinent evidence and arguments. "In reviewing the [E]xaminer's decision on appeal, the Board must necessarily weigh all of the evidence and argument." **Oetiker**, 977 F.2d at 1445, 24 USPQ2d at 1444. "[T]he Board must not only assure that the requisite findings are made, based on evidence of record, but must also explain the reasoning by which the findings are deemed to support the agency's conclusion." **In re Lee**, 277 F.3d 1338, 1344, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002).

With respect to dependent claims 40 and 45, Appellants argue at page 9 of the Appeal Brief that Mooney does not disclose a synchronous circuit as defined in the present application, nor does it teach the selection of an impedance from the driver circuit. Appellants further argue that Mooney provides no evidence of a motivation to modify the prior art to yield Appellants' claimed invention.

In order for us to decide the question of obviousness, "[t]he first inquiry must be into exactly what the claims define." **In re Wilder**, 429 F.2d 447, 450, 166 USPQ 545, 548 (CCPA 1970). "Analysis begins with a key legal question-- what is the invention claimed ?"...Claim interpretation...will normally

Appeal No. 2006-1204
Application No. 10/379,006

control the remainder of the decisional process." **Panduit Corp. v. Dennison Mfg.**, 810 F.2d 1561, 1567-68, 1 USPQ2d 1593, 1597 (Fed. Cir.), **cert. denied**, 481 U.S. 1052 (1987).

Appeal No. 2006-1204
Application No. 10/379,006

We note that independent claim 40 reads in part as follows:

"a synchronous circuit capable of providing a signal indicative of an impedance mismatch between the driver circuit and the load; and a controller for selecting one of the first plurality of impedances to reduce the impedance mismatch in response to the signal."

Thus, the claim does require a synchronous circuit and the selection of an impedance from the driver circuit.

We agree with Appellants, as noted in the discussion of claim 13 above, that Mooney does not teach a synchronous circuit as defined in the present application, nor does it teach a controller for selecting one of the first plurality of impedances to reduce the impedance mismatch in response to the signal. We further agree with Appellants that Mooney does not provide any motivation to modify the prior art in order to yield the claimed invention.

It is our view, after consideration of the record before us, that the evidence relied upon and the level of skill in the particular art would not have suggested to one of ordinary skill in the art the invention as set forth in claims 40 and 45. Accordingly, we will not sustain the Examiner's rejection of claims 40 and 45.

Appeal No. 2006-1204
Application No. 10/379,006

CONCLUSION

In view of the foregoing discussion, we have not sustained the Examiner's decision rejecting claims 1, 2, 5, 9-11, 13, 14, 22, 24, 25, 50 and 55 under 35 U.S.C. § 102. We have also not sustained the Examiner's decision rejecting claims 40 and 45 under 35 U.S.C. § 103. Therefore, we reverse.

REVERSED

KENNETH W. HAIRSTON)	
Administrative Patent Judge)	
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Appeal No. 2006-1204
Application No. 10/379,006

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