

The opinion in support of the decision being entered today was *not* written for publication and is *not* binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex Parte MINH V. NGO, NING CHENG, JEFF P. ERHARDT,
CLARENCE B. FERGUSON, CYRUS TABERY, JOHN CAFFALL,
TYAGAMOHAN GOTTIPATI and DAWN HOPPER

Appeal No. 2006-1208
Application No. 10/368,696

ON BRIEF

Before THOMAS, KRASS and JERRY SMITH, Administrative Patent Judges.

JERRY SMITH, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134 from the examiner's rejection of claims 1-20, which constitute all the claims pending in this application.

The disclosed invention pertains to a method of protecting charge trapping dielectric flash memory devices from UV-induced charging in Back-End-Of-Line (BEOL) processing.

Representative claim 1 is reproduced as follows:

1. A method of protecting a charge trapping dielectric flash memory cell from UV-induced charging, comprising:

- fabricating a charge trapping dielectric flash memory cell including a charge trapping dielectric charge storage layer in a semiconductor device; and
- during processing steps subsequent to formation of the charge trapping dielectric charge storage layer, protecting the charge trapping dielectric flash memory cell from exposure to a level of UV radiation sufficient to deposit a non-erasable charge in the charge trapping dielectric flash memory cell.

The examiner relies on the following references:

Shirota et al. (Shirota)	5,519,246	May 21, 1996
Kuo	6,417,053	July 9, 2002

The following rejection is on appeal before us:

1. Claims 1-20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the teachings of Shirota in view of Kuo.

Rather than repeat the arguments of appellants or the examiner, we make reference to the briefs and the answer for the respective details thereof.

OPINION

We have carefully considered the subject matter on appeal, the rejection advanced by the examiner and the evidence of obviousness relied upon by the examiner as support for the rejection. We have, likewise, reviewed and taken into consideration, in reaching our decision, the appellants' arguments set forth in the briefs along with the examiner's rationale in support of the rejection and arguments in rebuttal set forth in the examiner's answer.

It is our view, after consideration of the record before us, that the evidence relied upon by the examiner does not support the examiner's rejection. Accordingly, we reverse.

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the examiner to establish a factual basis to support the legal conclusion of obviousness. See In re Fine, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the examiner is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (1966). The examiner must articulate reasons for the examiner's decision. In re Lee, 277 F.3d 1338, 1342, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002). In particular, the examiner must show that there is a teaching, motivation, or suggestion of a motivation to combine references relied on as evidence of obviousness. Id. at 1343. The examiner cannot simply reach conclusions based on the examiner's own understanding or experience - or on his or her assessment of what would be basic knowledge or common sense. Rather, the examiner must point to some concrete evidence in the record in support of these findings." In re Zurko, 258 F.3d 1379, 1386, 59 USPQ2d 1693, 1697 (Fed. Cir. 2001). Thus the examiner must not only assure that the requisite findings are made, based on evidence of record, but must also explain the reasoning by which the findings are deemed to support the examiner's conclusion. However, a suggestion, teaching, or motivation to combine the relevant prior art teachings does not have to be found explicitly in the prior art, as the teaching, motivation, or suggestion may be implicit from the prior art as a whole, rather than expressly stated in the references. The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the

problem to be solved as a whole would have suggested to those of ordinary skill in the art.

In re Kahn, 441 F.3d 977, 987, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006) citing In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313 (Fed. Cir. 2000). See also In re Thrift, 298 F.3d 1357, 1363, 63 USPQ2d 2002, 2008 (Fed. Cir. 2002). These showings by the examiner are an essential part of complying with the burden of presenting a prima facie case of obviousness. Note In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). If that burden is met, the burden then shifts to the applicant to overcome the prima facie case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole and the relative persuasiveness of the arguments. See Id.; In re Hedges, 783 F.2d 1038, 1039, 228 USPQ 685, 686 (Fed. Cir. 1986); In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984); and In re Rinehart, 531 F.2d 1048, 1052, 189 USPQ 143, 147 (CCPA 1976). Only those arguments actually made by appellants have been considered in this decision. Arguments which appellants could have made but chose not to make in the brief have not been considered and are deemed to be waived [see 37 CFR § 41.37(c)(1)(vii)(2004)].

We now consider the examiner's rejection of claims 1-20 that stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the teachings of Shirota in view of Kuo. Since appellants' arguments with respect to this rejection have treated these claims as a single group which stand or fall together, we will consider independent claim 1 as the representative claim for this rejection.

We note at the outset that Shirota is directed to an Erasable Programmable Read Only Memory (EPROM) that has a portion of the memory reserved as a special information memory cell (i.e., the UPROM portion) that is protected from erasure by an “ultraviolet impermeability resin film” that also functions as an electrical insulator [Shirota, cols. 1 and 2].

EPROM devices are nonvolatile as they retain information even when power to the device is disconnected or interrupted. Once programmed, an EPROM device may be bulk erased by a timed exposure to an ultraviolet light source that directs ultraviolet (UV) light into the EPROM device through a transparent lid or window located on the integrated circuit enclosure. The exposure to UV light erases the EPROM by neutralizing the electrical charge on the floating gate of each cell.

Kuo teaches a fabrication method for a silicon Nitride Read-Only Memory (NROM) that is a flash memory device. Flash memory devices are specialized types of Electrically Erasable Programmable Read-Only Memory (EEPROM or E²PROM) devices. Like EPROM devices, EEPROM devices and flash memory EEPROM devices are nonvolatile. Unlike EPROM devices that require UV light for erasure, EEPROM devices are electrically erasable. Typically, EEPROM devices are erasable byte by byte. As set forth in the instant specification, a flash memory device differs from prior art EEPROM devices in that all the memory cells [or designated blocks] of a flash memory device may be erased using a single electrical current pulse [specification, page 1]. NROM devices resolve a current leakage problem with prior art floating gate flash memory EEPROM devices by using a “charge-

trapping layer” to replace the polysilicon floating gate [Kuo, col. 1, lines 23-61]. In addition, NROM devices have the advantage of storing two discrete charges or “bits” of memory in a single cell, thus realizing a much higher density memory device [Kuo, col. 1, line 65].

The Kuo patent is directed to solving the problem of preventing charges generated in the plasma process from being conducted to (and thereby possibly damaging or programming) the silicon Oxide/ silicon Nitride / silicon Oxide (ONO) composite layer during the manufacturing process. Damage (or programming) may result from the “antenna effect” where charges generated in the plasma process propagate along the metal interconnects [Kuo, col. 2, lines 14-21, lines 35-42]. Kuo addresses the “antenna effect” problem by implementing a “metal protection line” that essentially shunts the buildup of charges to the grounding doped region in the substrate to prevent damage (or programming) to the ONO composite layer [Kuo, col. 2, lines 35-67].

Kuo’s approach is presented as an improvement over the prior art diode-based approach for discharging transient charges that required a lower input voltage with an associated decrease in the speed of the writing operation [Kuo, col. 2, lines 27-32]. After fabrication, Kuo teaches the “metal protection line” is burned out with a high current, this process achieving the desired result of allowing a higher input voltage to be applied to the device to realize the advantage of faster write operations [Kuo, col. 2, lines 22-32, 62-67].

We note that appellants repeatedly refer in the brief to Shirota as teaching floating gate flash memory cells [e.g., brief, page 6]. However, the Shirota patent is silent with respect to teaching any type of electrically erasable “flash” memory device. Although both

EPROMs and flash memory EEPROMs utilize a floating gate component in the memory cell, they are different devices. The UV-erasable EPROM device taught by Shirota is not a “flash” device, because it is not an EEPROM that can be quickly erased with a single current pulse. It typically takes at least several minutes (or longer) to erase a UV-erasable EPROM device, depending upon the exact wavelength and intensity of the ultraviolet light source. We note that Shirota is silent with respect to the problem of UV light depositing a non-erasable charge on a memory cell. While Shirota does teach that UV rays are used to purposely erase EPROM floating gate memory cells, such erasure can be reversed by simply reprogramming the EPROM.

The examiner relies upon Shirota (fig. 1) as teaching a process of forming an ultraviolet impermeable resin film (1) over a nonvolatile memory device. The examiner acknowledges that Shirota does not explicitly teach fabricating a charge-trapping dielectric charge storage layer in a semiconductor device. The examiner asserts that it would have been obvious to one of ordinary skill in the art to substitute the floating gate structure in the process of Shirota with the charge-trapping dielectric charge storage layer taught by Kuo in order to resolve the current leakage problem associated with a polysilicon floating gate [answer, page 3].

The examiner further asserts that because Shirota in view of Kuo teaches a UV impermeable layer, the combined process is capable of protecting the charge-trapping dielectric flash memory layer from exposure to a level of UV radiation sufficient to deposit a non-erasable charge [answer, page 7]. Finally, the examiner points to extrinsic evidence

[U.S. Pat. 5,714,412 to Liang et al., col. 5, lines 55-62], not relied upon in the rejections, as supporting the contention that Back-End-Of-Line (BEOL) processes are well known in the art [answer, page 7].

Appellants point out that the instant specification discloses that exposure to UV is not a problem for floating gate devices [see specification, page 3, lines 13-17], and such devices are purposely exposed to UV radiation to neutralize any charge that builds up during processing [brief, page 7]. Appellants admit that it is well known in the art that UV radiation may be used to erase floating gate nonvolatile memory cells [brief, page 6].

If a proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). The motivation proffered by the examiner (i.e., to resolve the current leakage problem associated with a polysilicon floating gate) is a motivation for one of ordinary skill in the art to use a charge-trapping layer to replace the polysilicon floating gate of a prior art EEPROM flash memory device, as set forth by Kuo [col. 1, lines 17-60]. We note that the intended purpose of a UV-erasable EPROM device, as taught by Shirota [col. 1, lines 13-14], does not include rapid erasure of the device as is the case with the electrically erasable flash memory devices disclosed by Kuo [col. 1, lines 18, 36]. We note that if all the memory cells of the hypothetical combined “Shirota + Kuo” device were protected with the ultraviolet impermeable resin film of Shirota (as applied to protect the charge-trapping dielectric flash memory cells taught by Kuo), the intended purpose of reserving a dedicated non-erasable

(UPROM) section of the device, as taught by Shirota, would be defeated, as the hypothetical “Shirota + Kuo” combination “flash” memory device would have ALL memory cells subject to erasure by a single electrical pulse. Because Shirota teaches a floating gate UV-erasable EPROM device (and not a floating gate EEPROM flash memory device of the type disclosed by Kuo) we agree with appellants that one of ordinary skill in the art would not have been motivated to modify Shirota with the teaching of Kuo for the reason suggested by the examiner.

The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. In re Vaeck, 947 F.2d 488, 493, 20 USPQ2d 1438, 1442, (Fed. Cir. 1991). It is impermissible to use a claimed invention as a “template or guide” in order to piece together the teachings of prior art references which show only individual elements of the claimed invention in an effort to create a mosaic of such prior art to argue obviousness. In re Fritch, 972 F.2d 1260, 1265-6, 23 USPQ2d 1780, 1783-4 (Fed. Cir. 1992). “Determination of obviousness cannot be based on the hindsight combination of components selectively culled from the prior art to fit the parameters of the patented invention. There must be a teaching or suggestion within the prior art, or within the general knowledge of a person of ordinary skill in the field of the invention, to look to particular sources of information, to select particular elements, and to combine them in the way they were combined by the inventor.” ATD Corp. v. Lydall, Inc., 159 F.3d 534, 546, 48 USPQ2d 1321, 1329 (Fed. Cir. 1998).

As pointed out by appellants, it is the instant specification that discloses that a non-erasable charge can be deposited in the charge storage layer of a charge-trapping dielectric flash memory cell when the cell is exposed to UV radiation, [specification, page 3, lines 4-20, see also brief, page 7].

The examiner relies upon Kuo for its teaching of a charge-trapping dielectric storage layer in a flash memory cell [answer, page 3]. Because Kuo is silent with respect to the use of ultraviolet light for any purpose, and because Shirota is silent with respect to the problem of UV light depositing a non-erasable charge on a memory cell, as discussed *supra*, we agree with appellants that one of ordinary skill in the art would not have been aware of this problem by relying upon the cited references alone, without relying upon the disclosure of the instant specification.

In summary, we agree with appellants' contention that there is no reasonable teaching found in the references to motivate one of ordinary skill in the art to combine the UV-erasable EPROM device taught by Shirota with the electrically erasable flash NROM device of Kuo, except to protect Kuo's device from ultraviolet exposure during fabrication to prevent the formation of a non-erasable charge in the charge-trapping dielectric memory cell, and this teaching is only taught by the instant specification.

For at least the aforementioned reasons, we agree with appellants that the examiner has failed to meet his burden of presenting a *prima facie* case of obviousness. In summary,

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we will not sustain the examiner's rejection of any of the claims on appeal. Accordingly, the decision of the examiner rejecting claims 1-20 is reversed.

REVERSED

Comment [COMMENT1]: The year should be entered here.

JAMES D. THOMAS
Administrative Patent Judge

ERROL A. KRASS
Administrative Patent Judge

JERRY SMITH
Administrative Patent Judge

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