

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Ex parte JEAN-LUC NAULEAU, JANOS ERDELYI, and WILLIAM H. MCCALPIN

Appeal No. 2006-1657
Application No. 10/121,570

ON BRIEF

Before KRASS, JERRY SMITH, and RUGGIERO, Administrative Patent Judges.

JERRY SMITH, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1-30 and 50-53. Pending claims 31-49 have been withdrawn from consideration by the examiner. The examiner has now indicated that claims 2-5, 9, 12-30, 52, and 53 contain allowable subject matter [answer, page 2]. Therefore, this appeal is now directed to the rejection of claims 1, 6-8, 10, 11, 50 and 51.

The disclosed invention pertains to a system and apparatus for digital control of bias for transistors.

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Representative claims 1 and 10 are reproduced as follows:

1. A bias control device for biasing at least one transistor, the device having a transistor bias control unit comprising:

- a first digital to analog converter (DAC), including a software writable first register for converting a coarse bias control value in the first register to produce a first analog bias signal; and
- a buffer coupled to the first DAC for producing a bias control signal.

10. A bias power control system, the system comprising:

- a local control bus;
- a bias control device having a first register for storing a coarse bias control value, where the first register is software writable, a first digital to analog converter (DAC) coupled to the first register for converting the coarse bias control value to produce a first analog bias signal, and a buffer coupled to the first DAC for producing a bias control signal, the bias control device being coupled to the local control bus; and
- a controller being coupled to a memory and having a first interface for communicating with the local control bus, the controller being configured to write the coarse bias control value to the first register of the bias control device under the control of a program stored in the memory.

The examiner relies on the following reference:

Renzel et al. (Renzel)

4,373,394

Feb. 15, 1983

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The following rejection is on appeal before us:

1. Claims 1, 6-8, 10, 11, 50 and 51 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Renzel.

Rather than repeat the arguments of appellants or the examiner, we make reference to the briefs and the answer for the respective details thereof.

OPINION

We have carefully considered the subject matter on appeal, the rejection advanced by the examiner and the evidence of anticipation relied upon by the examiner as support for the rejection. We have, likewise, reviewed and taken into consideration, in reaching our decision, the appellants' arguments set forth in the briefs along with the examiner's rationale in support of the rejection and arguments in rebuttal set forth in the examiner's answer. Only those arguments actually made by appellants have been considered in this decision. Arguments which appellants could have made but chose not to make in the briefs have not been considered and are deemed to be waived. See 37 C.F.R. § 41.37(c)(1)(vii)(2004). See also In re Watts, 354 F.3d 1362, 1368, 69 USPQ2d 1453, 1458 (Fed. Cir. 2004).

It is our view, after consideration of the record before us, that the evidence relied upon supports the examiner's rejection of the claims on appeal. Accordingly, we affirm.

We consider the anticipation of the following logical groups of claims, as argued separately by appellants in the briefs:

GROUP I: Claims 1, 8 and 50 [brief, page 10].

GROUP II: Claims 6 and 7 [brief, pages 12-14; reply brief, page 2].

GROUP III: Claims 10 and 51 [brief, pages 12 - 14].

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GROUP IV: Claim 11 [brief, page 13; reply brief, page 14, ¶1].

In rejecting claims under 35 U.S.C. §102, a single prior art reference that discloses, either expressly or inherently, each limitation of a claim invalidates that claim by anticipation.

Perricone v. Medicis Pharmaceutical Corp., 432 F.3d 1368, 1375-6, 77 USPQ2d 1321, 1325-6 (Fed. Cir. 2005), citing Minn. Mining & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc., 976 F.2d 1559, 1565, 24 USPQ2d 1321, 1326 (Fed. Cir. 1992). To establish inherency, the extrinsic evidence “must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill.” Continental Can Co. v. Monsanto Co., 948 F.2d 1264, 1268, 20 USPQ2d 1746, 1749 (Fed. Cir. 1991). “Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.” In re Robertson, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999) (internal citations omitted). “Every element of the claimed invention must be literally present, arranged as in the claim.” Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989) (internal citations omitted).

GROUP I, claims 1, 8 and 50

I. We consider first the examiner’s rejection of claims 1, 8 and 50 as being anticipated by Renzel. Since Appellants’ arguments with respect to this rejection have treated these claims as a single group which stand or fall together, we will consider independent claim 1 as the representative claim for this rejection. See 37 C.F.R. § 41.37(c)(1)(vii)(2004).

(a) Appellants argue that transistors T₁ and T₂ are not driven by the output of operation amplifier 68 that the examiner relies upon as teaching the claimed buffer [brief, page 11].

Therefore, appellants conclude that the Renzel reference does not teach a bias control signal generated for biasing at least one transistor, as recited in claim 1 [*id.*].

In response, the examiner points out that Renzel teaches the circuit provides an output from operation amplifier 68 (fig. 2) for biasing transistor T₀ [answer, page 7, ¶3].

At the outset, we agree with appellants that transistors T₁ and T₂ (figs. 2 and 3) are not driven (i.e., biased) by the output of operation amplifier 68. However, we note that the examiner also points to the biasing of transistor T₀ (fig. 3) in the rejection of claim 1 [answer, page 4]. We agree with the examiner that the signal output of operational amplifier 68 that is applied to the base of transistor T₀ does, in fact, provide a “bias control signal” to transistor T₀, as claimed [claim 1]. We note that Renzel discloses that transistor T₀ functions to minimize the effect of the constant current I on operational amplifier 68, thus transistor T₀ is biased at its base by the current output of operational amplifier 68 [col. 5, lines 53-59; see also col. 8, lines 32-33]. We further note that Renzel explicitly discloses that operational amplifier 68 biases transistor T₀ at col. 9, lines 53-56:

The foregoing will result in amplifier 68 providing an output signal which biases transistor T₀ to the point where substantially no current will flow through resistor R₀ [emphasis added].

(b) Appellants argue that the examiner’s construction of the term “biasing” is so overbroad that it essentially applies to any voltage applied to a transistor junction [see 2nd reply brief, received Dec. 12, 2005, page 2, ¶1].

“During patent examination, the pending claims must be given their broadest reasonable interpretation consistent with the specification.” In re Hyatt, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000). The broadest reasonable interpretation of the claims must also be

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consistent with the interpretation that those skilled in the art would reach. In re Cortright, 165 F.3d 1353, 1358, 49 USPQ2d 1464, 1467 (Fed. Cir. 1999). Claim terms are presumed to have the ordinary and customary meanings attributed to them by those of ordinary skill in the art. Sunrace Roots Enterprise Co. v. SRAM Corp., 336 F.3d 1298, 1302, 67 USPQ2d 1438, 1441 (Fed. Cir. 2003); Brookhill-Wilk 1, LLC. v. Intuitive Surgical, Inc., 334 F.3d 1294, 1298, 67 USPQ2d 1132, 1136 (Fed. Cir. 2003) (“In the absence of an express intent to impart a novel meaning to the claim terms, the words are presumed to take on the ordinary and customary meanings attributed to them by those of ordinary skill in the art.”).

In the instant case, we find that Renzel uses the term “biases” in accordance with the plain, ordinary and accustomed meaning that one of ordinary skill in the art would clearly understand as being applied to the base (or gate) of a transistor device [Renzel, col. 9, lines 53-56]. Therefore, we do not agree with appellants that the examiner’s construction of the term “biasing” is so overbroad that it essentially applies to any voltage applied to a transistor junction [see 2nd reply brief, received Dec. 12, 2005, page 2, ¶1].

We note that a transistor device must necessarily be biased to be operational, regardless of whether the transistor functions as a switch (i.e., biased in cutoff or saturation), or as an amplifier (i.e., biased at a “Q” or quiescent operating point). We further find that this particular line of argument by appellants improperly reads limitations from the specification into the claims [e.g., see 2nd reply brief, page 3, ¶3]. We note that appellants also argue that the instant invention performs an adjustment of the bias signal for a transistor as the transistor ages [*id.*]. A basic canon of claim construction is that one may not read a limitation into a claim from the written description. Renishaw plc v. Marposs Societa’ per Azioni, 158 F.3d 1243, 1248, 48 USPQ2d

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1117, 1120 (Fed. Cir. 1998). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. In re Van Geuns, 988 F.2d 1181, 1184, 26 USPQ2d 1057, 1059 (Fed. Cir. 1993). Patentability is based upon the claims. “It is the claims that measure the invention.” SRI Int’l v. Matsushita Elec. Corp., 775 F.2d 1107, 1121, 227 USPQ 577, 585 (Fed. Cir. 1985) (en banc). When making a patentability determination, the claimed invention must be compared to the prior art [*id.*, emphasis added]. In the instant case, we note that biasing a transistor in its active or linear region (i.e., by setting the bias at the transistor’s “Q” or quiescent operating point) is not claimed.

We also agree with the examiner that non-inverting operational amplifier 68 provides a buffer coupled to the analog output of D/A converter 42 (i.e., corresponding to the claimed “first digital to analog converter (DAC)”) [claim 1]. Therefore, we agree with the examiner that Renzel teaches all of the recited structural elements, arranged as claimed.

(c) Appellants further argue that Renzel discloses a sawtooth waveform generator for use in display devices, such as an oscilloscope, and not the claimed bias control device for biasing at least one transistor [brief, page 12, ¶2].

In response, the examiner notes that appellants appear to be arguing the language found in the preamble of claim 1 [answer, page 6]. The examiner asserts that the “transistor bias control unit” recited in the preamble is merely stating the intended purpose or use of the circuit, and therefore all that is required is that the prior art be capable of providing the intended use or function [*id.*].

“The effect preamble language should be given can be resolved only on review of the entirety of the patent to gain an understanding of what the inventors actually invented and

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intended to encompass by the claim.” Corning Glass Works v. Sumitomo Elec. U.S.A., Inc., 868 F.2d 1251, 1257, 9 USPQ2d 1962, 1966 (Fed. Cir. 1989). However, “[i]f the body of the claim sets out the complete invention,” then the language of the preamble may be superfluous. Schumer v. Lab. Computer Sys., Inc., 308 F.3d 1304, 1310, 64 USPQ2d 1832, 1837 (Fed. Cir. 2002); Bristol-Myers Squibb Co. v. Ben Venue Labs., Inc., 246 F.3d 1368, 1373-74, 58 USPQ2d 1508, 1512 (Fed. Cir. 2001). A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See In re Hirao, 535 F.2d 67, 70, 190 USPQ 15, 17 (CCPA 1976) and Kropa v. Robie, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951). In the instant case, we note that there is no “transistor” recited in the body of claim 1 to support the language set forth in the preamble. Therefore, we agree with the examiner that the language of the preamble of claim 1 is merely a statement of intended purpose or use. Accordingly, to show anticipation, the examiner, as finder of fact, need only show that the prior art structure is capable of performing the intended purpose or function.

In response to appellants’ argument that Renzel’s invention is not directed to appellants’ intended purpose of controlling transistor biasing, we recognize that Renzel discloses a circuit that functions as a sawtooth waveform generator for use in display devices, such as an oscilloscope [brief, page 12, ¶1; see also Renzel col. 2, lines 16-25]. However, we note that the Court of Appeals for the Federal Circuit has determined that the absence of a disclosure relating to function does not defeat a finding of anticipation if all the claimed structural limitations are found in the reference. In re Schreiber, 128 F.3d 1473, 1477, 44 USPQ2d 1429, 1431 (Fed. Cir.

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1997). In Schreiber, the court held that a funnel-shaped oil dispenser spout anticipated a claimed conical-shaped popcorn dispensing top, even though the function of popcorn dispensing was not taught by the reference, because the reference met all the structural limitations of the claim. In re Schreiber, 128 F.3d at 1479, 44 USPQ2d 1429 at 1433.

In the instant case, we find that the Renzel reference does teach all the structural elements arranged as claimed, as discussed *supra*. We also agree with the examiner that Renzel's disclosed structure is capable of performing the instant intended purpose or function of controlling transistor biasing. Accordingly, because the absence of a disclosure relating to an intended use or function does not defeat a finding of anticipation, we will sustain the examiner's anticipation rejection of representative claim 1 for essentially the same reasons argued by the examiner. Because dependent claims 8 and 50 are not argued separately, we will also sustain the examiner's rejection of these claims.

GROUP II, claims 6 and 7

II. We next consider the examiner's rejection of claims 6 and 7 as being anticipated by Renzel. Since Appellants' arguments with respect to this rejection have treated these claims as a single group which stand or fall together, we will consider dependent claim 6 as the representative claim for this rejection. See 37 C.F.R. § 41.37(c)(1)(vii)(2004).

Appellants argue that the examiner cites no teaching for the claimed digital interface device configured to interface with a system bus as recited in claim 6 [brief, page 12, ¶3]. Appellants further argue that decoder 76 is incapable of writing data to memory 74 because there is no data path from decoder 76 to memory 74 via data bus 64 [2nd reply brief, received Dec. 27, 2005, page 4, ¶1].

In response, the examiner contends that decoder 76 of Renzel is a digital interface device that interfaces with a system bus [answer, page 8]. The examiner states that decoder 76 receives a software message from microprocessor 62 and writes data from the microprocessor to a software writable register, i.e., memory 74 [answer, page 8; see also Renzel, fig. 2].

We note that Renzel explicitly discloses that bus 64 is a “data bus” and bus 66 is a “control or address bus” [col. 5, lines 18 and 19]. We agree with appellants that fig. 2 shows no data path from decoder 76 to memory 74 via data bus 64. Therefore, we agree with appellants that decoder 76 cannot receive a software message from microprocessor 62 on bus 64 (i.e., the data bus) in the manner argued by the examiner. We find that decoder 76 functions primarily as an address decoder that simply maps memories 70 and 74 and counter 36 into the address space of microprocessor 62.

However, we note that Renzel discloses that decoder 76 provides an additional function. In particular, Renzel explicitly discloses that decoder 76 also controls the clearing of storage devices 70 and 74. See col. 6, lines 65-68:

The clearing and loading of storage devices 70 and 74 and counter 36 is under the control of the output of a decoder 76 which is connected to bus 66 and thus is controlled by the output of microprocessor 62 [emphasis added].

Therefore, we do not agree with appellants that decoder 76 is incapable of writing data to memory 74 because there is no data path connecting decoder 76 to memory 74 via data bus 64. In particular, we find that the clearing function disclosed by Renzel is equivalent to writing data to these memory devices (i.e., by clearing all memory or register bits). We note that a value of all zeros in a register of memory 74 will be converted to a corresponding zero reference \underline{U}_E

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output voltage by D/A converter 42 that is supplied as an input to non-inverting operational amplifier 68 that further biases transistor T₀, as disclosed by Renzel:

See Renzel at col. 5, lines 53-59:

The operational amplifier 68 is connected as a non-inverting amplifier and, in combination with resistor R₀, functions as a constant current source. The current I provided by amplifier 68 is a function of the magnitude of the input signal U_E applied thereto from converter 42 and the size of resistor R₀.

See Renzel at col. 9, lines 53-56:

The foregoing will result in amplifier 68 providing an output signal which biases transistor T₀ to the point where substantially no current will flow through resistor R₀ [emphasis added].

Thus, transistor T₀ functions as a switch (i.e., transistor T₀ is biased at its gate either in cutoff or saturation by the output of operational amplifier 68). We further note that the recited “system bus” is broadly but reasonably construed as encompassing a data bus, an address bus, or a control bus. We further find that the recited “software message” broadly reads upon a control signal, such as a control signal that clears or resets a storage device or register, as discussed *supra*. Accordingly, we will sustain the examiner’s rejection of representative claim 6. Because dependent claim 7 is not argued separately, we will also sustain the examiner’s rejection of claim 7.

GROUP III, claims 10 and 51

III. We next consider the examiner’s rejection of claims 10 and 51 as being anticipated by Renzel. Since Appellants’ arguments with respect to this rejection have treated these claims as a single group which stand or fall together, we will consider independent claim 10 as the representative claim for this rejection. See 37 C.F.R. § 41.37(c)(1)(vii)(2004).

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Appellants argue that Renzel does not teach a controller as recited in claim 10 [brief, page 12, ¶3, see also page 13, ¶3]. Appellants assert that decoder 76 is not a controller [*id.*]. Appellants further argue that the examiner fails to cite any support to show that decoder 76 operates under program control [brief, page 13, ¶2].

In response, the examiner essentially restates the argument previously set forth with respect to claim 6 regarding the control function of decoder 76 [answer, page 8]. The examiner also notes that it is notoriously well known that a microprocessor is a device that operates under the control of a program [answer, page 9].

We note again that Renzel explicitly discloses that decoder 76 controls not only counter 36 but also the clearing and loading of storage devices 70 and 74, as discussed *supra* with respect to claim 6 [Renzel, col. 6, lines 65-68]. In particular, we note that Renzel explicitly discloses that decoder 76 is controlled by the output of microprocessor 62 [col. 6, line 68]. Since microprocessor 62 operates under program control, we find that decoder 76 also operates under program control by virtue of being controlled by microprocessor 62.

In the alternative, we note that the claimed “controller” also broadly reads upon microprocessor 62, as shown in fig. 2 operatively coupled as claimed [Renzel, fig. 2]. We further note that microprocessor 62 inherently operates under the control of a program stored in memory, as claimed [fig. 2]. Accordingly, we will sustain the examiner’s rejection of representative claim 10 for essentially the same reasons argued by the examiner. Because dependent claim 51 has not been argued separately, we will also sustain the examiner’s rejection of claim 51.

GROUP IV, claim 11

IV. Lastly, we consider the examiner's rejection of claim 11 as being anticipated by Renzel.

Appellants argue that Renzel does not teach a controller configured to retrieve the coarse bias control value from memory in order to write it to the first register of the bias control device [brief, page 14, ¶1].

In response, the examiner argues that the value on bus 64 is stored in the first register responsive to decoder 76 being controlled by the microprocessor [answer, page 8]. The examiner further argues that the claim is silent with respect to what value the "control value" is "coarse" with respect to [*id.*]. The examiner asserts that the "control value" provided in memory 74 would be considered "coarse" with respect to some arbitrary value [*id.*].

We note that the examiner asserts in the rejection that the claimed "coarse bias control value" is stored in memory 46 within microprocessor 62 and this value is then applied to memory 74 and further applied as an input to D/A converter 42 [answer, page 5]. We further note that Renzel discloses that a digital code (i.e., a "nominal" or coarse "set-point value") is stored in memory 46 [col. 4, lines 43-56]. We note that Renzel teaches that a preliminary "coarse" setting is obtained by means of microprocessor selection of capacitors C1-C8 (fig. 2) in further combination with an average control voltage value \underline{U}_E (fig 2) that is a function of the initial number loaded into memory 74 that is further supplied as an input value to D/A converter 42 [Renzel, col. 6, lines 50-55].

We agree with the examiner that the claim is silent with respect to what value the recited "control value" is coarse with respect to, and therefore it is reasonable to conclude that the "control value" provided in memory 74 would be considered "coarse" with respect to some

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arbitrary value [claim 11]. We find that the recited term “coarse” is extremely broad in scope (we note that this discussion is also applicable to independent claim 10, *supra*). Therefore, we agree with the examiner that the claim broadly reads upon the Renzel reference in the manner suggested by the examiner. Accordingly, we will sustain the examiner’s rejection of dependent claim 11.

In summary, we have sustained the examiner’s rejection of all claims on appeal. Therefore, the decision of the examiner rejecting claims 1, 6-8, 10, 11, 50 and 51 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

ERROL A. KRASS
Administrative Patent Judge

JERRY SMITH
Administrative Patent Judge

JOSEPH F. RUGGIERO
Administrative Patent Judge

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FRANCISSSEN PATENT LAW, P.C.
53 W. JACKSON
SUITE #656
CHICAGO, IL 60604