

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ALONGKORN KITAMORN, ASHWINI KULKARNI,
GORDON D. MCINTOSH, KANISHA PATEL, and MICHAEL ANTHONY PEREZ

Appeal No. 2006-1757
Application No. 10/116,522

ON BRIEF

Before HAIRSTON, JERRY SMITH, and HOMERE, Administrative Patent Judges.

JERRY SMITH, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134 from the examiner's rejection of claims 1-27, which constitute all the claims pending in this application.

The disclosed invention pertains to locating hardware faults in multiple devices in a data processing system. Specifically,

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the devices are scanned in a particular order to analyze any possible error condition. When a new error is detected in a device, an identification of the device is stored in a data structure. When the devices are subsequently scanned, the system will skip over those devices whose identity has been stored in the data structure.

Representative claim 1 is reproduced as follows:

1. A method comprising:

detecting an error in a first device from a plurality of devices, wherein the plurality of devices is associated with a scanning order; and

scanning information regarding the plurality of devices in the scanning order to identify the first device, skipping over each device that is identified in a data structure.

The examiner relies on the following reference:

Cepulis et al (Cepulis) 6,496,945 Dec. 17, 2002
(filed Jun. 4, 1998)

The following rejection is on appeal before us:

Claims 1-27 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Cepulis.

Rather than repeat the arguments of appellants or the examiner, we make reference to the briefs and the answer for the respective details thereof.

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OPINION

We have carefully considered the subject matter on appeal, the rejection advanced by the examiner and the evidence of anticipation relied upon by the examiner as support for the rejection. We have, likewise, reviewed and taken into consideration, in reaching our decision, the appellants' arguments set forth in the briefs along with the examiner's rationale in support of the rejection and arguments in rebuttal set forth in the examiner's answer.

It is our view, after consideration of the record before us, that the disclosure of Cepulis fully meets the invention as set forth in the claims on appeal. Accordingly, we affirm.

Anticipation is established only when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of a claimed invention as well as disclosing structure which is capable of performing the

recited functional limitations. RCA Corp. v. Applied Digital Data Systems, Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir.); cert. dismissed, 468 U.S. 1228 (1984); W.L. Gore and Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 1554, 220 USPQ

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303, 313 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984).

Only those arguments actually made by appellants have been considered in this decision. Arguments which appellants could have made but chose not to make in the briefs have not been considered and are deemed to be waived [see 37 CFR § 41.37(c) (1) (vii) (2004)].

The examiner has indicated how the claimed invention is deemed to be fully met by the disclosure of Cepulis [answer, pages 3-6]. Regarding independent claim 1,¹ appellants argue that Cepulis does not disclose "skipping over each device that is identified in a data structure" as claimed [brief, page 11]. In this regard, appellants contend that block 202 in the flow chart shown in Fig. 2 of Cepulis (clearing out the logical resource map) actually prevents skipping over each device identified in a

data structure as claimed [brief, page 13]. According to appellants, because the logical resource map only comes into existence at the end of the flowchart (i.e., step 216) and no other processes or steps follow this step, the recited skipping cannot occur during any activity in Cepulis' flowchart [id.].

¹ Appellants indicate that independent claim 1 is representative of the first

The examiner responds that Cepulis identifies and skips faulty devices by only permitting access to those devices that are listed as available in the logical resource map [answer, page 7]. In this regard, the examiner notes that Cepulis at block 216 indicates what devices are available -- and therefore, by implication, what is not available [id]. The examiner also notes that although the logical resource map is cleared at step 202, it is nevertheless repopulated based on the contents of the failed device log 132 [id]. Appellants respond that Cepulis' permitting access to devices listed as available is opposite to the claimed skipping step. Moreover, "logical devices listed as available," according to appellants, is opposite to the scanning step recited in claim 1 [reply brief, page 2].

Regarding claims 8, 17, and 26, appellants argue that Cepulis' non-volatile RAM (NVRAM) 130 that stores the failed device log does not disclose an error register as claimed [brief, pages 14 and 15]. Specifically, appellants contend that "NVRAM is not known to use registers" [brief, page 15]. The examiner responds that registers are intrinsic to NVRAM devices, particularly the type of NVRAM that Cepulis uses (*i.e.*, EEPROMs or

battery backed-up RAM) [answer, page 8].

We will sustain the examiner's anticipation rejection. At the outset, we note that steps 204, 206, and 208 in Fig. 2 of Cepulis fully meet the limitation of claim 1 calling for "scanning information regarding the plurality of devices in the scanning order to identify the first device." After initially clearing the logical resource map, Cepulis sequentially obtains ID codes of failed devices from the failed device log. The system then tags as unavailable those logical resources that correspond to the failed physical devices [Cepulis, Fig. 2, step 212]. Based on this tagging process, only available logical devices are reported to the computer's operating system [Cepulis, Fig. 2, step 216].

In our view, Cepulis' method of reporting only those logical devices that are available (*i.e.*, logical resources that are not tagged as unavailable) reasonably constitutes "skipping over each device that is identified in a data structure" as claimed. Specifically, tagging unavailable resources corresponding to failed physical devices inherently identifies such failed devices in a data structure. Moreover, reporting only available devices to the operating system inherently "skips over" (*i.e.*, omits) the

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unavailable devices.

We are unpersuaded by appellants' argument that step 202 (clearing the logical resource map) prevents the claimed skipping step. As the examiner indicates, step 202 merely clears the logical resource map, but the map is repopulated each time the method of flow chart 200 is executed. In short, Cepulis' sequential tagging of logical resources corresponding to failed devices and reporting only devices that are available in step 216 reasonably constitutes skipping over identified failed devices. Claim 1 is therefore fully met by Cepulis.

Regarding claims 8, 17, and 26, we also agree with the examiner that registers are intrinsic to the types of NVRAM devices used to store the failed device log in Cepulis (e.g., an EEPROM or battery backed-up RAM). We find unpersuasive appellants' assertion that "NVRAM is not known to use registers" on page 15 of the brief. There is simply no evidence on this record to support appellants' assertion. Such unsupported statements are tantamount to mere lawyer's arguments and conclusory statements that, when unsupported by factual evidence,

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are entitled to little probative value. In re Geisler, 116 F.3d 1465, 1470, 43 USPQ2d 1362, 1365 (Fed. Cir. 1997); In re De Blauwe, 736 F.2d 699, 705, 222 USPQ 191, 196 (Fed. Cir. 1984); In re Wood, 582 F.2d 638, 642, 199 USPQ 137, 140 (CCPA 1978); In re Lindner, 457 F.2d 506, 508-09, 173 USPQ 356, 358 (CCPA 1972). On the other hand, ample factual evidence exists to support the examiner's position that certain NVRAM devices inherently contain registers.² The examiner's anticipation rejection of claims 8, 17, and 26 based on the disclosure of Cepulis is proper and is therefore sustained.

Since appellants have not separately argued the patentability of dependent claims 2-7, 9, 11-16, 18, 20-25, and 27, these claims fall with independent claims 1, 10, and 19. See In re Nielson, 816 F.2d 1567, 1572, 2 USPQ2d 1525, 1528 (Fed. Cir. 1987). See also 37 CFR § 41.37(c) (vii).

In summary, we have sustained the examiner's rejection with respect to all claims on appeal. Therefore, the decision of the examiner rejecting claims 1-27 is affirmed.

² See, e.g., U.S. Pat. Re. 38,660, col. 10, lines 11-16 (noting that a micro-controller can access registers in an EEPROM); U.S. Pat. 6,708,273, col. 72, line 38 - col. 73, line 45 (describing EEPROM registers); U.S. Pat. 6,043,943, col. 3, lines 31-34 (noting that registers 28 can comprise dedicated permanent memory such as an EEPROM).

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No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a)(1)(iv).

AFFIRMED

KENNETH W. HAIRSTON)
Administrative Patent Judge)
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) BOARD OF PATENT
JERRY SMITH)
Administrative Patent Judge)
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) APPEALS AND
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