

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte HECTOR TORRES, MARK W. MORGAN

and JULIE HWANG

Appeal No. 2006-1816
Application No. 10/386,146

ON BRIEF

Before HAIRSTON, SAADAT, and MACDONALD, Administrative Patent Judges.
SAADAT, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134(a) from the Examiner's final rejection of claims 1, 2, 5-8, 10 and 12-15. Claims 3, 4, 9, 11 and 16-18 have been indicated as allowable.

We affirm-in-part.

BACKGROUND

Appellants' invention is directed to a high-speed front-multiplexed repeater circuit that limits input leakage current levels in the event one or more input voltages of the circuit exceeds the supply voltage. The multiplexor includes a plurality of transmission gates made of a first PMOS pass transistor and an NMOS pass transistor (specification, page 3). The first blocking element is coupled between the supply voltage and the back-gate nodes of the first PMOS transistors while a second blocking element is coupled between the gate nodes of the first PMOS transistors and the source nodes of the NMOS transistors (id.). According to Appellants, a first diode blocks the back-gate leakage to the supply voltage and the second blocking element blocks the leakage current paths from the differential inputs to the first PMOS transistors when the PMOS transistor is "off" and an input voltage exceeds the supply voltage (id.). An understanding of the invention can be derived from a reading of exemplary independent claim 1, which is reproduced below:

1. A driver circuit, comprising:

a plurality of differential inputs;

at least one differential output;

a plurality of control inputs; and

a multiplexor coupled between the differential inputs and the at least one differential output, the multiplexor being configurable by the control inputs to allow a selected one of the differential inputs to be routed to at least one differential output, the

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multiplexor including a plurality of transmission gates, each transmission gate including a first pass transistor corresponding to a respective signal path of one of the differential inputs,

wherein the multiplexor further includes at least one first blocking element coupled between a back-gate node of each first pass transistor and a supply voltage to block a first leakage current path from the back-gate node to the supply voltage, and at least second blocking element coupled between a gate node of each first pass transistor and the respective signal path corresponding thereto to block a second leakage current path from the respective signal path to the first pass transistor.

The Examiner relies on the following prior art references:

Ko 5,955,912 Sep. 21, 1999

Graves et al. (Graves) 6,100,719 Aug. 8, 2000

Claims 1, 2, 5-8, 10, 12-15 and 17¹ stand rejected under the second paragraph of 35 U.S.C. § 112 as being indefinite.

Claims 1, 2, 5-8, 10, 12-15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ko and Graves.

¹The Examiner's indication of allowability of claim 17 appears to have been intended in absence of rejection based on prior art.

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We make reference to the briefs and answer for the respective positions of Appellants and the Examiner. Only those arguments actually made by Appellants have been considered in this decision. Arguments which Appellants could have made but chose not to make in the briefs have not been considered (37 CFR § 41.37(c)(1)(vii)).

OPINION

With respect to the 35 U.S.C. § 112 rejection of the claims, the Examiner questions the clarity of the second blocking element and finds such limitation to be misdescriptive since transistor MP5 is merely a shunt transistor and cannot block when activated (answer, page 3). Appellants argue that it is not necessary that the transistor MP5 block in all circumstances but its needs to block some of the times in accordance with the control signal V_{CDM} (brief, page 3). Appellants argue that since transistor MP5 has blocking characteristics, it is not misdescriptive (*id.*). In response, the Examiner indicates that the transistor is only a clamping transistor and the only blocking is done by blocking element D0 (answer, page 6).

Upon a careful review of the claim language and the specification, we find that although the transistor MP5 is connected as a shunt across the source nodes of the respective NMOS transistors and gate nodes of PMOS transistors of the transmission

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gates and clamps the gate-to-source voltages (specification, page 11, lines 11-24), it blocks the back-gate leakage to the power supply (specification, page 12, lines 10-19). It is clear from the specification as a whole, and the above noted excerpts specifically, that although diode D0 through node CHP is connected to the back-gate node of transistor MP5, it still functions as a blocking element to prevent the input current from flowing into the first pass transistor MP1.

In view of the above and in light of the specification as a whole, we find that the MP5 transistor is sufficiently defined as a blocking element and would reasonably apprise those skilled in the art of the scope of this limitation. Accordingly, we will not sustain the rejection of claims 1, 2, 5-8, 10, 12-15 and 17 under the second paragraph of 35 U.S.C. § 112.

Turning now to the 35 U.S.C. § 103 rejection of the claims, we note that the Examiner has indicated how the claimed invention is deemed to be obvious over the modified teachings of Ko to include the first and the second blocking elements D7 and MP3 of Graves, as depicted in Figure 1 (answer, pages 3-4). Appellants argue that Graves relates to a low voltage bus switch circuit for isolation under power down conditions and has nothing to do with multiplexors (brief, page 4). The Examiner responds that since

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Appellants' diode D0 is the only blocking element for both the first and the second elements, the claimed blocking elements read on diode D7 of Graves (answer, pages 6-7).

As a general proposition, in rejecting claims under 35 U.S.C. § 103, the examiner bears the initial burden of presenting a prima facie case of obviousness. See In re Rijckaert, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993) and In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). A prima facie case of obviousness is established when the teachings of the prior art itself would appear to have suggested the

claimed subject matter to one of ordinary skill in the art. See In re Bell, 991 F.2d 781, 783, 26 USPQ2d 1529, 1531 (Fed. Cir. 1993); In re Fritch, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992); Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir. 1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985).

From our review of Ko and Graves, we remain unpersuaded by Appellants' arguments that any error in the Examiner's

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determination regarding the obviousness of the claimed subject matter has occurred. Ko describes a multiplexor circuit including the transmission gates and differential inputs and outputs. See Figures 4-6. Graves on the other hand teaches a low-voltage bus switch that prevents leakage during the power loss and thus maintains the isolation of the bus (col. 2, lines 5-15). Although Graves does not mention a multiplexor structure, the disclosed switch pertains to isolation of circuitry and preventing leakage which is missing in Ko. Graves further discloses the complementary pass transistors MN1 and MP1 and

diode D7 as the first blocking element between the back-gate of the first pass transistor MP1 and a power supply (col. 3, lines 47-55). Although the Examiner considers both blocking elements as the blocking diode D0 connected to the power supply, Graves clearly shows the claimed second blocking element as the blocking transistor MP3 which is coupled between a gate node of the first pass transistor MP1 and a respective signal path such as that of the input terminal B for preventing a current leakage from the input terminal through the first pass transistor to the output (col. 3, lines 8-22).

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We observe that Appellants have not disputed any other teachings of Graves and its combinability with Ko, nor have provided any arguments with respect to any other claims. Therefore, as the Examiner has established a *prima facie* case of obviousness with respect to claim 1, we sustain the **35 U.S.C. § 103(a) rejection of claim 1, as well as claims 2, 5-8, 10, 12-15, as falling together** (brief, page 5), over Ko and Graves.

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CONCLUSION

In view of the foregoing, the decision of the Examiner rejecting claims 1, 2, 5-8, 10, 12-15 and 17 under 35 U.S.C. § 112 is reversed, but is affirmed with respect to the rejection of claims 1, 2, 5-8, 10, 12-15 under 35 U.S.C. § 103.

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No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

KENNETH W. HAIRSTON Administrative Patent Judge))))))	BOARD OF PATENT APPEALS AND INTERFERENCES
MAHSHID D. SAADAT Administrative Patent Judge)))	
ALLEN R. MACDONALD Administrative Patent Judge))	

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