

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte PETER HAZUCHA
and KRISHNAMURTHY SOUMYANATH

Appeal No. 2006-1901
Application No. 10/742,436

ON BRIEF

Before THOMAS, SAADAT, and HOMERE, Administrative Patent Judges.
SAADAT, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134(a) from the Examiner's final rejection of claims 1-3, 5-9 and 11. Claims 12-19 have been indicated as allowable while claims 4 and 10 have been objected to as being dependent upon a rejected claim, but otherwise allowable if rewritten to include all the limitations of their base claim and any intervening claims.

We affirm.

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BACKGROUND

Appellants' invention is directed to a method of protection against single event upsets (SEUs) in a latch circuit which may be caused by ionizing radiation. According to Appellants, protecting against SEUs restores a latch output to its original value or suppresses such transient signals (specification, page 4). An understanding of the invention can be derived from a reading of exemplary independent claim 1, which is reproduced below:

1. A latch circuit, comprising:

a first latch; and

a second latch to harden the latch circuit to a single event upset, the second latch including a transmission gate including two transistors, the transmission gate having an output port to couple to only one transistor of the first latch.

The Examiner relies on the following prior art references:

Jamshidi et al. (Jamshidi) 5,646,558 Jul. 8, 1997

Zhang 6,026,011 Feb. 15, 2000

T. Calin et al. (Calin), "Upset Hardened Memory Design for Submicron CMOS Technology," IEEE Transactions on Nuclear Science, Vol. 43, No. 6, December 1996, pp. 2874-2878.

Claims 1-3, 7-9 and 11 stand rejected under 35 U.S.C.

§ 103(a) as being unpatentable over Calin and Jamshidi.

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Claims 1-3, 5 and 6 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Zhang and Jamshidi.

We make reference to the briefs and answer for the respective positions of Appellants and the Examiner. Only those arguments actually made by Appellants have been considered in this decision. Arguments which Appellants could have made but chose not to make in the briefs have not been considered (37 CFR § 41.37(c)(1)(vii)).

OPINION

In rejecting claims 1-3, 7-9 and 11, the Examiner relies on Calin or Zhang for teaching a latch circuit comprising first and second latches and the transmission gate in the second latch (answer, pages 3-5). The Examiner further relies on Jamshidi for providing a two-transistor transmission gate to be used instead of the transmission gate with a single transistor as described in Calin (answer, page 4). Relying on Jamshidi's disclosure related to providing a full signal swing by using two transistors, the Examiner concludes that using two transistors in the transmission gate of Calin would have been obvious to one of ordinary skill in the art (id.).

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Appellants argue that there is no motivation for combining the references because both Jamshidi and Zhang teach away from dual transistor designs in order to avoid increasing the die area (brief, page 10). In particular, Appellants point out that Jamshidi actually is related to eliminating dual transistor design in a pass gate as it increases die area and power dissipation (brief, page 11). Appellants further provide arguments related to increased die area if the complementary pass gate of Jamshidi is used in the latch design of Calin or Zhang and conclude that no reasonable expectation of success supports the combination (id.).

In response to Appellants' arguments, the Examiner asserts that using two transistors as the transfer gate, while taking up more space, enhances the circuit reliability and minimizing the failure rate (answer, page 5). With respect to Appellants' argument regarding the lack of reasonable expectation of success, the Examiner argues that the combination would be desirable since it does increase the circuit reliability even though it is at the expense of using more of the chip's real estate (answer, page 8). The Examiner adds that one skilled in the art would have been willing to trade circuit size for a better performance if keeping the chip area small results in inadequate performance (id.).

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As a general proposition, in rejecting claims under 35 U.S.C. § 103, the examiner bears the initial burden of presenting a prima facie case of obviousness. See In re Rijckaert, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993) and In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). A prima facie case of obviousness is established when the teachings of the prior art itself would appear to have suggested the claimed subject matter to one of ordinary skill in the art. See In re Bell, 991 F.2d 781, 783, 26 USPQ2d 1529, 1531 (Fed. Cir. 1993); In re Fritch, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992); Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir. 1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985). In considering the question of the obviousness of the claimed invention in view of the prior art relied upon, the Examiner is expected to make the factual determination set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), and to provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. See also In re Rouffet, 149

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F.3d 1350, 1355, 47 USPQ2d 1453, 1456 (Fed. Cir. 1998). However, the motivation, suggestion or teaching may come explicitly from statements in the prior art, the knowledge of one of ordinary skill in the art, or, in some cases the nature of the problem to be solved. See In re Dembiczak, 175 F.3d 994, 999, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999).

From our review of Calin and Jamshidi, we find that both references provide sufficient motivation for using two transistors in a latch circuit when a higher level of reliability is desired. In particular, Jamshidi describes complementary switch pass gates having the advantage of allowing the voltage at common node to swing the full logic values with the loading of the common node as its disadvantage (col. 1, lines 66 through col. 2, line 3). Additionally we observe that Calin teaches the use of storage latch duplication and state-restoring feedback circuits as viable design hardening techniques while recognizing high chip area overhead and high power dissipation as its drawbacks (page 2874). However, Calin points out that such drawbacks may be tolerated in situations where reliability prevails over the cost of increased die area (page 2874, last paragraph of right hand column). Thus, contrary to Appellants'

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assertion that Calin teaches away from the combination (brief, page 10), the reference actually recognizes the trade off between reliability and die size and how each may have priority based on the application.

We also agree with the Examiner (answer, page 8) that reduction in die size, as suggested by Calin, although may increase reliability at the expense of larger die size, does not necessarily make the device inoperative. Although we recognize that a reference teaches away from combination if combination produces seemingly inoperative device, see In re Gordon, 733 F.2d 900, 902, 221 USPQ 1125, 1127(Fed. Cir. 1984), the instant combination merely presents different parameters needed for the desired characteristics of the device. In fact, the combination of Calin and Jamshidi produces smaller capacity in exchange for more reliable performance where reliability is more important than speed or die size without making the device inoperative.

We also find Appellants' arguments based on increasing die area (brief, page 11 & reply brief, page 2) to be unpersuasive, if not irrelevant as no such limitations are recited, since increasing the die size or power dissipation is also recognized by both Calin (page 2874) and Zhang (col. 5,, lines 2-5) in cases

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where reliability is not of the same concern as dies area or speed. Here, the relevant inquiry is whether there is a reason, suggestion, or motivation in the prior art that would lead one of ordinary skill in the art to combine the teachings of the references, and that would also suggest a reasonable likelihood of success (In re Kotzab, 217 F.3d 1365, 1369-70, 55 USPQ2d 1313, 1316-17 (Fed. Cir. 2000)). After weighing the arguments presented by Appellants and the Examiner and the disclosure of Calin, Zhang and Jamshidi, we find that the combination of the prior art, as a whole is sufficient to establish obviousness based on increasing reliability even though the die area may be larger.

Therefore, we remain unpersuaded by Appellants' arguments that any error in the Examiner's determination regarding the obviousness of the claimed subject matter has occurred. Accordingly, as the Examiner has established a prima facie case of obviousness with respect to claim 1, we sustain the 35 U.S.C. § 103(a) rejection of claim 1, as well as claims 2, 3, 7-9 and 11, argued as one group, over Calin and Jamshidi.

Turning now to the rejection of claims 1-3, 5 and 6, we note that Appellants' arguments in support of patentability of these

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claims include assertions similar to those addressed above with respect to claim 1 (brief, pages 10-12). We are unpersuaded that the combination of Jamshidi with Zhang, as set forth by the Examiner (answer, page 4-6 & 8). As such, and for the reasons similar to those underlying our conclusion with respect to claim 1, we find that the Examiner has set forth a reasonable case of prima facie obviousness and the 35 U.S.C. § 103 rejection of claims 1-3, 5 and 6 over Zhang and Jamshidi should be sustained.

CONCLUSION

In view of the foregoing, the decision of the Examiner rejecting claims 1-3, 5-9 and 11 under 35 U.S.C. § 103 is affirmed.

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No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a)(1)(iv).

AFFIRMED

JAMES D. THOMAS)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
MAHSHID D. SAADAT)	APPEALS
Administrative Patent Judge)	AND INTERFERENCES
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