

The opinion in support of the decision being entered today was *not* written for publication and is *not* binding precedent of the Board.

**UNITED STATES PATENT AND TRADEMARK OFFICE**

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**BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES**

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*Ex parte* Dipankar Bhattacharya, Makeswar Kothandaraman, John Christopher Kriz,  
Bernard Lee Morris, Jeffrey Jay Nagy, and Stefan Allen Siegel,

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Appeal No. 2006-2034  
Application No. 10/744,801

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ON BRIEF

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Before HAIRSTON, BARRY, and MACDONALD, *Administrative Patent Judges*.

BARRY, *Administrative Patent Judge*.

A patent examiner rejected claims 1, 18, and 25. The appellants appeal therefrom under 35 U.S.C. § 134(a). We reverse.

I. BACKGROUND

The invention at issue on appeal concerns compensating a circuit for variations. Circuit desirers often employ high speed buffers to meet demands for speed and performance in integrated circuits ("ICs"). Variations in the performance of buffers over different process, voltage, and temperature ("PVT") ranges, however, have impeded the design of faster buffers. (Spec. at 1.)

Accordingly, the appellants' invention generates compensation signals based on characteristic information from both PMOS and NMOS devices. The PMOS and NMOS devices used to generate the compensation signal are matched to one or more PMOS and NMOS devices in the IC to be compensated such that the compensation signals track PVT variations in the circuit. (*Id.* at 2.)

A further understanding of the invention can be achieved by reading the following claim.

1 . A compensation circuit, comprising:

a reference circuit including a reference NMOS device and a reference PMOS device, the reference circuit being operative to generate a first reference signal and a second reference signal, the first reference signal being a function of at least one of a process characteristic, a voltage characteristic and a temperature characteristic of the reference NMOS device, and the second reference signal being a function of at least one of a process characteristic, a voltage characteristic and a temperature characteristic of the reference PMOS device, the reference circuit being configured to provide the first and second reference signals as separate and independent outputs; and

a control circuit connected to the reference circuit, the control circuit being operative to receive the first and second reference signals and to generate one or more output signals for compensating for a variation in at least one of a process characteristic, a voltage characteristic and a temperature characteristic of at least one NMOS device and at least one PMOS device in a circuit to be compensated, which is connectable to the control circuit, in response to the first and second reference signals, respectively.

Claims 1, 18, and 25 stand rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 6,349,060 ("Ogura").

## II. OPINION

"It is essential that the Board be provided with a brief fully stating the position of the appellant with respect to each ground of rejection presented for review in the appeal so that no search of the record is required in order to determine that position. Thus, the brief should not incorporate or reference previous responses." M.P.E.P. § 1205.02 (8th ed., Rev. 3 Aug. 2005). Here, the appellant's principal brief attempts to "incorporate by reference . . . the disclosures of all previous responses filed in the present application, namely, responses dated May 20, 2005 and September 27, 2005." (App. Br. at 5.) Such an attempt to incorporate previous responses is inappropriate and will be disregarded. Only the positions stated in the appellants' briefs will be considered.

"Rather than reiterate the positions of the examiner or the appellant *in toto*, we focus on the main point of contention therebetween." *Ex parte Sehr*, No. 2003-2165, 2005 WL 191041, at \*2 (Bd.Pat.App & Int. 2004). The examiner finds, "The equation  $I_5 = m_2 \cdot I_1$  is dependent upon the characteristics of transistor 206 being similar to the characteristics of transistor 181.  $I_5$  would vary if the process characteristic or

temperature characteristic of transistor 206 was changed." (Examiner's Answer at 5.)

He also alleges, "The current I4 is a function of at least of [sic] the process characteristic of transistor 304 because the value of I4 will vary if the characteristic of transistor 304 were changed." (*Id.*) The appellants argue, "In accordance with the teachings of Ogura and contrary to the Examiner's contentions, the current I4 in sense amplifier 22 is based on the characteristics of an NPN bipolar transistor rather than on characteristics of an NMOS . . . transistor device." (Reply Br. at 2.)

"In addressing the point of contention, the Board conducts a two-step analysis. First, we construe the independent claims at issue to determine their scope. Second, we determine whether the construed claims are anticipated." *Ex parte Wang*, No. 2003-0513, 2004 WL 4978835, at \*2 (Bd.Pat.App & Int. 2004).

#### A. CLAIM CONSTRUCTION

"Analysis begins with a key legal question — what is the invention claimed?"

*Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561, 1567, 1 USPQ2d 1593, 1597 (Fed. Cir. 1987). Here, independent claim 1 recites in pertinent part the following limitations:

the reference circuit being operative to generate a first reference signal and a second reference signal, the first reference signal being a function of at least one of a process characteristic, a voltage characteristic and a temperature characteristic of the reference NMOS device, and the second reference signal being a function of at least one of a process

characteristic, a voltage characteristic and a temperature characteristic of the reference PMOS device. . . .

Independent claim 18 includes similar limitations. In other words, the limitations require a reference signal that is a function of at least one of a process characteristic, a voltage characteristic, and a temperature characteristic of an NMOS device and another reference signal that is a function of at least one of a process characteristic, a voltage characteristic and a temperature characteristic of a PMOS device.

#### B. ANTICIPATION DETERMINATION

"Having construed the claim limitations at issue, we now compare the claims to the prior art to determine if the prior art anticipates those claims." *In re Cruciferous Sprout Litig.*, 301 F.3d 1343, 1349, 64 USPQ2d 1202, 1206 (Fed. Cir. 2002). "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros., Inc. v. Union Oil Co.*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987) (citing *Structural Rubber Prods. Co. v. Park Rubber Co.*, 749 F.2d 707, 715, 223 USPQ 1264, 1270 (Fed. Cir. 1984); *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548, 220 USPQ 193, 198 (Fed. Cir. 1983); *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 771, 218 USPQ 781, 789 (Fed. Cir. 1983)). "[A]bsence from the reference of any claimed

element negates anticipation." *Kloster Speedsteel AB v. Crucible, Inc.*, 793 F.2d 1565, 1571, 230 USPQ 81, 84 (Fed. Cir. 1986).

Here, in Ogura "[a] flash memory having a sense amplifier is provided with a constant-current source having the positive temperature characteristic and a constant-current source having the negative temperature characteristic." (Abs. at ll. 1-4.) "FIG. 4 is a circuit diagram representing th[is] arrangement. . . ." (Col. 8, l. 56.) In this arrangement, the "sense amplifier 22 is provided with P-channel MOS transistors 205 and 206 for supplying a verifying sense amplifier load current. . . ." (*Id.* at ll. 60-62.) Because the Figure shows that the PMOS transistor supplies the load current I5, we agree with the examiner's finding that I5 constitutes a reference signal that is a function of at least one of a process characteristic, a voltage characteristic and a temperature characteristic of a PMOS device.

As aforementioned, the examiner equates Ogura's I4 current with the claim's reference signal that is a function of at least one of a process characteristic, a voltage

characteristic, and a temperature characteristic of an NMOS device. For its part, the reference teaches that the constant current I4 is provided by the following equation:

$$I_4 = \frac{V_2}{R_2} = \frac{2V_{be}}{R_2}$$

In the equation,  $R_2$  is the resistance value of resistor 309, and  $V_{be}$  is "the diffusion voltage of transistors 306 and 307," (col. 9, ll. 16-17), which are "NPN transistors. . . ." (*Id.* at l. 11.) Because the reference's constant current I4 is a function of characteristics of a resistor and two NPN transistors, rather than a characteristic of an NMOS transistor, we disagree with the examiner's allegation that I4 constitutes a reference signal that is a function of at least one of a process characteristic, a voltage characteristic and a temperature characteristic of an NMOS device.

The absence of a reference signal that is a function of at least one of a process characteristic, a voltage characteristic, and a temperature characteristic of an NMOS device negates anticipation. Therefore, we reverse the anticipation rejection of claims 1 and 18 and of claim 25, which depends from the former claim.

### III. CONCLUSION

In summary, the rejection of claims 1, 18, and 25 under § 102(b) is reversed.

REVERSED

KENNETH W. HAIRSTON  
Administrative Patent Judge

LANCE LEONARD BARRY  
Administrative Patent Judge

ALLEN R. MacDONALD  
Administrative Patent Judge

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