

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte WILLIAM A. HARRIS

Appeal No. 2006-2332
Application No. 09/751,610

ON BRIEF

Before THOMAS, HAIRSTON, and BLANKENSHIP, Administrative Patent Judges.

BLANKENSHIP, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1-3, 20-24, 26-29, 31-37, 39-45, 47, and 48, which are all the claims remaining in the application.

We affirm.

BACKGROUND

The invention relates to electronic control systems, in particular precision phase generators for generating multiple phase clocking signals from a single phase clock signal. Representative claim 20 is reproduced below.

20. A method for generating at least two clock signals displaced from each other by a predetermined phase shift of $360^\circ/2N$, where N is a positive integer, the method comprising:

applying a clock signal to a signal input of a phase lock loop circuit at a desired clock frequency;

applying a feedback signal to a second input of the phase lock loop circuit;

generating an output signal of the phase lock loop circuit having a frequency of $2NF_0$;

coupling the output signal of the phase lock loop circuit to a clock input of each JK flip-flop of a Johnson counter to provide the feedback signal to the second input of the phase lock loop circuit having a frequency corresponding to the frequency of the output signal of the phase lock loop circuit divided by $2N$, the Johnson counter comprising N JK flip-flops including an input JK flip-flop, an output JK flip-flop, and a plurality of middle JK flip-flops, each JK flip-flop having a J input, a K input, the clock input, a Q output, and a complemented Q output, each middle JK flip-flop and the output JK flip-flop having its J input coupled to the Q output of a preceding JK flip-flop and its K input coupled to the complemented Q output of the preceding JK flip-flop, the J input of the input JK flip-flop being coupled to the complemented Q output of the output JK flip-flop, the K input of the input JK flip-flop being coupled to the Q output of the output JK flip-flop; and

coupling outputs of the JK flip-flops of the Johnson counter for use as phase shifted clock outputs.

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The examiner relies on the following references:

Epstein	4,093,870	Jun. 6, 1978
Li	5,058,132	Oct. 15, 1991

M. Morris Mano (Mano), Computer Engineering Hardware Design 130-32, Prentice-Hall, Inc. (1988).

Claims 1-3, 20-24, 26-29, 31-37, 39-45, 47, and 48 stand rejected under 35 U.S.C. § 103 as being unpatentable over Li, Epstein, and Mano.

We refer to the Final Rejection (mailed Apr. 28, 2005) and the Examiner's Answer (mailed Mar. 13, 2006) for a statement of the examiner's position and to the Brief (filed Jan. 9, 2006) and the Reply Brief (filed May 11, 2006) for appellant's position with respect to the claims which stand rejected.

OPINION

Based on appellant's arguments in the Brief, we will select claim 20 to decide the appeal from the rejection that is applied against all of the claims. See 37 CFR § 41.37(c)(1)(vii).

The examiner finds that Li describes a circuit (Fig. 2) for dividing an input clock signal into N (N=5) clock signals having a relative phase separation of $360/2N$, the circuit including a phase lock loop circuit 102 in the general arrangement as claimed. The examiner further finds that Li describes a Johnson counter (114; Fig. 2) comprised of five flip-flops to make up five stages, referring to column 5, lines 50 through 64 of Li.

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The examiner also finds that Li does not disclose that the Johnson counter has N JK flip-flops in the particular arrangement required by claim 20. The rejection turns to Epstein's Figure 4 as disclosing a Johnson counter using JK flip-flops consistent with the claimed arrangement. Mano is further relied upon as teaching the reliability of JK flip-flops. The examiner concludes that it would have been obvious to implement the five stage Johnson counter described by Li with a five JK flip-flop circuit arranged in accordance with the teachings of Epstein. (Answer at 3-4.)

Appellant submits there is no prior art evidence of a suggestion for combining the references, nor evidence of a reasonable expectation of success of the combination. Appellant notes that Epstein's Johnson counter has only three flip-flops. Mano does not discuss Johnson counters, or the relative merits of different Johnson counters. (Brief at 13.) Neither Li nor Epstein shows a Johnson counter having an input JK flip-flop, an output JK flip-flop, and "a plurality of middle" JK flip-flops (i.e., a minimum of four JK flip-flops) as claimed. As for the "reasonable expectation of success," appellant submits there is no evidence of how the elements of Li, Epstein, and Mano are to be arranged and assembled together. (Id. at 14.)

Appellant further argues that column 5 of Li describes the Johnson counter as a divide by ten, five bit shift register. According to appellant, there is no suggestion in Li that a Johnson counter may be fabricated from JK flip-flops, and although Epstein shows a Johnson counter the counter has only three JK flip-flops. (Reply Brief at 5.)

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In our view, the examiner has provided evidence sufficient to show prima facie obviousness of the subject matter as a whole of instant claim 20. Li does not show or otherwise describe the details of the five bit shift register that comprises Johnson counter 114. We find that the combination of Li and Epstein would have suggested using five JK flip-flops to effect the Johnson counter that is taught by Li. The suggestion from the prior art for the combination is as basic as suggesting how the artisan should construct the Johnson counter described by Li. The suggestion to combine may come from the prior art, as filtered through the knowledge of one skilled in the art. Motorola, Inc. v. Interdigital Tech. Corp., 121 F.3d 1461, 1472, 43 USPQ2d 1481, 1489 (Fed. Cir. 1997); see also Cable Elec. Prods., Inc. v. Genmark, Inc., 770 F.2d 1015, 1025, 226 USPQ 881, 886-87 (Fed. Cir. 1985) (“[T]he suggestion to modify the art to produce the claimed invention need not be expressly stated in one or all of the references used to show obviousness. ‘Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art.’”) (quoting In re Keller, 642 F.2d 413, 425, 208 USPQ 871, 881).

With respect to the alleged lack of a “reasonable expectation of success,” the examiner has provided a reasonable basis for why the Johnson counter described by Li would be expected to operate if implemented with five JK flip-flops as suggested. If, in fact, the Li device would fail to operate within the scope of the method set forth by instant claim 20 if the Johnson counter were implemented with five JK flip-flops, appellant could have provided evidence, or at least a reasoned explanation based on

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the evidence of record, in support of the allegation. The allegation, without more, carries little weight in the instant inquiry.

Because Li and Epstein are sufficient to demonstrate prima facie unpatentability of at least instant claim 20, we consider Mano to represent merely cumulative teachings. We sustain the § 103 rejection of claims 1-3, 20-24, 26-29, 31-37, 39-45, 47, and 48.

CONCLUSION

The rejection of claims 1-3, 20-24, 26-29, 31-37, 39-45, 47, and 48 under 35 U.S.C. § 103 is affirmed.

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No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a). See 37 CFR § 1.136(a)(1)(iv).

AFFIRMED

JAMES D. THOMAS
Administrative Patent Judge

KENNETH W. HAIRSTON
Administrative Patent Judge

HOWARD B. BLANKENSHIP
Administrative Patent Judge

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