

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte WEN LING M. HUANG, JAMES KIRCHGESSNER, and DAVID MONK

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Appeal No. 2006-2525  
Application No. 10/178,672

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ON BRIEF

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Before HAIRSTON, BARRY, and BLANKENSHIP, Administrative Patent Judges.  
BLANKENSHIP, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's rejection of claims 3-9, which are all the claims remaining in the application.

We affirm.

BACKGROUND

The invention relates to integrated circuits that support digital circuits, analog circuits, and Radio-Frequency (RF) circuits on a single microchip. Representative claim 3 is reproduced below.

3. An integrated circuit, comprising:

a highly resistive substrate;

a patterned low resistivity buried layer formed directly on said highly resistive substrate, wherein said patterned low resistivity buried layer has a same conductivity type as said highly resistive substrate;

a digital circuit formed over said patterned low resistivity buried layer;

an analog circuit formed on said highly resistive substrate;

a passive RF device formed on said highly resistive substrate; and

an active RF device, wherein said active RF device is formed over said highly resistive substrate and is not formed over the patterned low resistivity buried layer.

The examiner relies on the following references:

Leipold et al. (Leipold) US 6,348,718 B1 Feb. 19, 2002  
(filed May 14, 1999)

Celler et al. (Celler) US 6,388,290 B1 May 14, 2002  
(filed Jun. 10, 1998)

Wong et al. (Wong) US 2002/0179977 A1 Dec. 5, 2002  
(effective filing date no later than Sep. 6, 2001)

Claims 3-7 stand rejected under 35 U.S.C. § 103 as being unpatentable over Celler and Leipold.

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Claims 8 and 9 stand rejected under 35 U.S.C. § 103 as being unpatentable over Celler, Leipold, and Wong.

We refer to the Rejection (mailed May 5, 2005) and the Examiner's Answer (mailed Mar. 20, 2006) for a statement of the examiner's position and to the Brief (filed Jan. 6, 2006) and the Reply Brief (filed May 18, 2006) for appellants' position with respect to the claims which stand rejected.

### OPINION

Based on appellants' arguments in the Brief, we will decide the appeal on the basis of rejected claim 3.<sup>1</sup> See 37 CFR § 41.37(c)(1)(vii).

The examiner finds that Celler teaches the subject matter of instant claim 3 except for a patterned low resistivity buried layer and the active RF device as it relates to the patterned low resistivity buried layer. Celler teaches a digital CMOS device (col. 4, ll. 4-6). Although not express in the statement of the rejection (Answer at 3-4), Celler also does not teach how the digital circuit might relate to a patterned low resistivity buried layer. The examiner further finds that Leipold teaches forming a patterned low resistivity buried layer, as specified by the claim, only beneath a digital CMOS circuit (e.g., under field effect transistors 12; Leipold Fig. 1). The examiner concludes that the

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<sup>1</sup> Appellants' remarks in response to the rejection of claims 8 and 9 rely on the argued deficiencies in the rejection applied against base claim 3.

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subject matter as a whole of instant claim 3 would have been obvious to one skilled in the art because Leipold teaches a patterned low resistivity layer within the requirements of the claim for the purpose of preventing undesirable latch-up effects in CMOS devices such as those taught by Celler.

Appellants submit that the rejection errs because Leipold teaches that the buried layer must be formed under all the active devices but not formed under any of the passive devices, referring to column 2, lines 26 through 28 of the reference. As such, in appellants' view, Leipold teaches that active devices must be formed over the patterned low resistivity buried layer (Brief at 4.) According to appellants, a combination of Celler and Leipold would require that the buried layer be under the active RF devices; otherwise, the teachings of Leipold would be destroyed. Leipold requires the buried layer to be under all of the active devices to prevent any latch-up effects, referring to column 2, lines 27 through 30. (Id. at 5.) Appellants further contend that the digital CMOS circuits 12, depicted in Figure 1 of the reference, are only examples of active circuits, referring to column 2, lines 20 through 22. As such, the digital CMOS circuits 12 represent all active devices. Appellants again note that Leipold teaches forming the buried layer "under the active components" to prevent a latch-up effect, referring to column 2, lines 26 through 30. (Id. at 6.)

The examiner responds that nowhere does Leipold state that the buried layer must be formed under all the active devices. According to the examiner, Leipold's teachings with respect to the conductive layer relate to latch-up effects, which are

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typical in CMOS chips. The “active components” described by Leipold are CMOS devices. The teachings of placement of the buried layer relate only to active CMOS components, in the examiner’s view. (Answer at 6-7.)

Appellants reiterate, in turn, the contention that Leipold teaches forming a buried layer under all active devices, whether CMOS or any other type. As for the teaching in Leipold that the buried layer prevents latch-up in CMOS devices, appellants posit that the prevention of latch-up is just one advantage of the buried layer if the active devices are CMOS devices, which is just one embodiment. Appellants refer again to column 2, lines 20 through 21 in support of the view that Leipold’s teachings relating to the buried layer are not limited to CMOS devices. (Reply Brief at 2.)

Leipold’s patent is entitled, “Integrated CMOS Circuit For Use At High Frequencies.” All the claims (1-7) specify an integrated CMOS circuit and active CMOS components. The first sentence of the patent states that “[t]he invention relates to an integrated CMOS circuit for use at high frequencies with active CMOS components and passive components.”

The text at column 1, lines 46 through 54 of Leipold appears, in our view, to relate that the buried layer created under active CMOS components prevents undesirable latch-up effects. Appellants seem to agree that latch-up effects are peculiar to CMOS circuits. (See, e.g., spec. at 2, 2nd ¶.) The text at column 2, lines 20 through 25 of Leipold, when read in context, seems to refer to CMOS components, or active CMOS components, rather than all active components. For example, Schottky diodes

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are described in a CMOS circuit in column 3, line 6 et seq. The text at column 2, lines 26 through 30 says that the conducting layer is formed under the active components, but the next sentence speaks of the layer preventing latch-up effects. The text thus appears to relate to active CMOS components, rather than any kind of active component.

What a reference teaches is a question of fact. In re Baird, 16 F.3d 380, 382, 29 USPQ2d 1550, 1552 (Fed. Cir. 1994); In re Beattie, 974 F.2d 1309, 1311, 24 USPQ2d 1040, 1041 (Fed. Cir. 1992). Upon consideration of the reference in its entirety, we conclude that Leipold provides ample support for the examiner's findings with respect to what the reference teaches. Appellants' arguments do not persuade us otherwise. We sustain the rejection of the claims on appeal because appellants have not demonstrated error in the examiner's case for *prima facie* obviousness.

### CONCLUSION

The rejection of claims 3-9 under 35 U.S.C. § 103 is affirmed.

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No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a). See 37 CFR § 1.136(a)(1)(iv).

AFFIRMED

KENNETH W. HAIRSTON )  
Administrative Patent Judge )  
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 ) BOARD OF PATENT  
LANCE LEONARD BARRY ) APPEALS  
Administrative Patent Judge ) AND  
 ) INTERFERENCES  
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HOWARD B. BLANKENSHIP )  
Administrative Patent Judge )

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FREESCALE SEMICONDUCTOR, INC.  
LAW DEPARTMENT  
7700 WEST PARMER LANE MD:TX32/PL02  
AUSTIN, TX 78729