The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte ALAN R. BALL, PAUL J. HARRIMAN, STEPHEN MEEK, and SUZANNE NEE

Appeal No. 2006-2920
Application No. 10/813,501

ON BRIEF

Before HAIRSTON, JERRY SMITH, and MACDONALD, Administrative Patent Judges.

JERRY SMITH, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134 from the examiner's rejection of claims 1-20.

The disclosed invention pertains to a method of forming a self-gated transistor and structure therefor.

Representative claim 1 is reproduced as follows:

1. A method of forming a self-gated transistor comprising:

- coupling a transistor operable to form a sense signal representative of a current through the self-gated transistor; and
- configuring a first circuit of the self-gated transistor to disable the transistor substantially upon a positive current flow through the transistor and to enable the transistor responsively to a negative current flow through the transistor.

The examiner relies on the following reference:

Asada et al. (Asada)	5,936,440	Aug. 10, 1999

The examiner relies on the following reference as extrinsic evidence to explain the operation of a comparator:

Millman et al. (Millman), Integrated Electronics: Analog and Digital Circuits and Systems 568 (1972).

The following rejection is on appeal before us:

1. Claims 1-20 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Asada [answer, pages 3-7].

Rather than repeat the arguments of appellants or the examiner, we make reference to the briefs and the answer for the respective details thereof.

OPINION

We have carefully considered the subject matter on appeal, the rejection advanced by the examiner and the evidence of anticipation relied upon by the examiner as support for the rejection. We have, likewise, reviewed and taken into consideration, in reaching our decision, the appellants' arguments set forth in the briefs along with the examiner's rationale in support of the rejection and arguments in rebuttal set forth in the examiner's answer. Only those arguments actually made by appellants have been considered in this decision. Arguments which appellants could have made but chose not to make in the briefs have not been considered and are deemed to be waived. See 37 C.F.R. § 41.37(c)(1)(vii)(2004). See also In re Watts, 354 F.3d 1362, 1368, 69 USPQ2d 1453, 1458 (Fed. Cir. 2004).

It is our view, after consideration of the record before us, that the evidence relied upon by the examiner does not support the examiner's rejection of claims 1-20. Accordingly, we reverse.

In rejecting claims under 35 U.S.C. § 102, a single prior art reference that discloses, either expressly or inherently, each limitation of a claim

invalidates that claim by anticipation. Perricone v. Medicis Pharmaceutical Corp., 432 F.3d 1368, 1375-6, 77 USPQ2d 1321, 1325-6 (Fed. Cir. 2005), citing Minn. Mining & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc., 976 F.2d 1559, 1565, 24 USPQ2d 1321, 1326 (Fed. Cir. 1992). To establish inherency, the extrinsic evidence "must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." Continental Can Co. v. Monsanto Co., 948 F.2d 1264, 1268, 20 USPQ2d 1746, 1749 (Fed. Cir. 1991). "Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." In re Robertson, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999) (internal citations omitted). To anticipate, every element and limitation of the claimed invention must be found in a single prior art reference, arranged as in the claim. Karsten Mfg. Corp. v. Cleveland Golf Co., 242 F.3d 1376, 1383, 58 USPQ2d 1286, 1291 (Fed. Cir. 2001); Scripps Clinic & Research Foundation v. Genentech, Inc., 927 F.2d 1565, 1576, 18 USPQ2d 1001, 1010 (Fed. Cir. 1991).

We consider first the examiner's rejection of claims 1-7 as being anticipated by Asada. Since Appellants' arguments with respect to this rejection have treated these claims as a single group which stand or fall

together, we will consider independent claim 1 as the representative claim for this rejection. See 37 C.F.R. § 41.37(c)(1)(vii)(2004).

Appellants argue that Asada fails to disclose the limitation of "configuring a first circuit of the self-gated transistor to disable the transistor substantially upon a positive current flow through the transistor," as claimed [brief, page 4; reply brief, page 5; see also claim 1, emphasis added]. With respect to the portions of the reference relied on by the examiner, appellants specifically argue that Asada's circuit of fig. 5 (and fig. 4) does not have a mode of operation that disables transistors 10 and 841 responsive to a positive current flow through transistor 10 [brief, page]. Appellants argue that Asada's circuit of fig. 5 (and fig. 4) disables transistors 10 and 841 responsive to the voltage Vs (and the current through resistor 801) being less negative than reference voltage Vr [brief, page].

The examiner disagrees [answer, page 7]. Specifically, the examiner notes that Asada discloses the reference voltage Vr is negative and nearly ground potential [id.; see Asada, col. 6, lines 21 and 22]. The examiner asserts that "nearly ground potential" is a potential equal to or very close to ground, e.g. less than 1/10 millivolt [answer, page 7]. The examiner asserts that the output of Asada's comparator 840 would not change state to turn off transistor 841 immediately after the voltage potential at its negative input terminal increases from a potential below Vr to a potential above Vr

because of the comparator input offset voltage [id.]. The examiner points to extrinsic evidence (see Millman non patent reference) as providing support for the contention that the voltage at the negative input terminal of Asada's comparator (i.e., Vs as shown in fig. 4) must be at least 1 millivolt above Vr in order for the output of the comparator to change state [id.]. The examiner further asserts that transistor 841 would not turn off immediately after the voltage potential at the comparator's negative input terminal increased from a potential below Vr to a potential above Vr because there are delays in Asada's second driving circuit 7 and NAND gate 501 [id.]. The examiner asserts that the comparator and the delays of second driving circuit 7 and NAND gate 501 create a voltage offset [id.]. The examiner asserts that the voltage at the negative input terminal of the comparator must be a positive voltage in order to turn OFF transistor 841 [id.]. The examiner further asserts that when the negative terminal of the comparator reaches a voltage above ground, the current flowing through transistor 841 is a positive current [answer, page 8]. The examiner concludes the "less negative voltage" referred to in Appellants' arguments that causes transistor 841 to turn off must be a positive voltage, and therefore Asada anticipates the limitations of claim 1 [answer, page 8; see also brief page 5].

At the outset, we note that for the purpose of this appeal we adopt the electrical engineering convention that positive current flows from positive to

negative voltage drop. With respect to the operation of the inductive load driving apparatus disclosed by Asada, we note that switching transistor 9 is turned ON when battery 2 has a low voltage and needs charging, as detected by comparator 53 that provides an output generation control signal Vc that indicates a low-battery condition by going HIGH [Asada, col. 4, lines 21-25]. We note that when transistor 9 is ON, field coil 32 is energized by the DC battery voltage to generate an electromagnetic field that induces a current flow in rotating three-phase armature winding 30 that charges the automobile battery after rectification by three-phase-full-wave rectifier 31 [id., see also col. 2, lines 56-60]. We note that when the battery is fully charged, generation control signal Vc goes LOW, turning OFF transistor 9 (which turns off the DC current applied to field coil 32), disabling the alternator charging voltage output [col. 4, lines 11-25]. We note that after a short delay, switching transistor 10 is turned ON to shunt the backflow current from field coil 32 to ground [col. 8, lines 4-18]. We note that when field coil 32 is turned OFF (i.e., not supplied with power through transistor 9), the battery charge cycle will not resume again until a low-battery condition is again detected by comparator 53, as indicated by generation control signal Vc again going HIGH [col. 3, lines 29-33]. We further note that Asada discloses if field coil voltage Vx is higher than ground level, the second driving circuit 7 turns off the low-side switching element 10 (i.e.,

transistor 10), irrespective of the level of generation control signal Vc [col. 6, lines 3-6].

With respect to the direction of current flow, we note that when transistor 9 is turned ON, a positive current flows from the positive battery 2 terminal through transistor 9 to power alternator field coil 32, (and thus enable the alternator to generate AC voltage), as shown in fig. 1. We note that the lower terminal of field coil 32 is connected to ground [fig. 1]. We note that when transistor 9 is ON and field coil 32 is energized (i.e., when the alternator is charging the battery) transistor 10 is turned OFF (i.e., disabled) and no current flows through transistor 10 [col. 5, line 66 through col. 6, line 3]. However, we note that when transistor 9 turns OFF (as controlled by first driving circuit 6 as further controlled by generation control signal Vc), a backflow current begins to flow in the reverse direction (i.e., from ground to a lower-than-ground voltage potential at the high-side terminal of field coil 32) as the electromagnetic field collapses immediately after the positive current flow that energizes field coil 32 is switched OFF by transistor 9 [col. 4, lines 4-10; col. 6, lines 24-31; col. 8, lines 4-18].

With respect to Asada's comparator 840 (figs. 4 and 5), we note that comparator 840 compares two voltage signals (i.e., Vs and Vr as shown in fig. 4) and determines which one is greater. The result of this comparison is indicated by output voltage Vd (fig. 4). We note that if the comparator's

output is saturated in the positive direction (i.e., comparator output = HIGH), this means that the non-inverting (+) input (Vr) has a greater, or more positive, voltage than the inverting (-) input voltage (Vs), (i.e., where all voltages measured with respect to ground). We further note that if the comparator's output voltage (Vd) is near the negative supply voltage (i.e., comparator output = LOW), it means that the inverting (-) input (Vs) has a greater, or more positive, voltage than the non-inverting (+) input voltage (Vr). Thus, the operation of comparator 840 (as shown in figs. 4 and 5) is described by Table 1:

TABLE 1

Comparator 840 input condition	Vd output of comparator
Vs < Vr	HIGH
Vs > Vr	LOW

We note that the above described operation of comparator 840 is supported at col. 6, lines 24-28, where Asada discloses that a HIGH level comparator output signal Vd is provided to NAND gate 502 when the voltage drop Vs (across resistor 800) becomes lower than reference voltage Vr, and

further, that this condition turns ON transistor 10. Significantly, we note that the question before us turns upon the recognition that Asada's comparator 840 changes state when both input voltages are negative with respect to ground potential, AND one input voltage crosses the other input voltage (i.e., Vs < Vr or Vs > Vr). In particular, we note that negative voltages have associated negative currents with respect to ground potential.

With respect to the operation of Asada's second driving circuit 7 (as shown in detail in fig. 1 and in block form in figs 4 and 5), we note that when generation control signal Vc goes HIGH (i.e., indicating a low battery condition), transistor 10 (i.e., low-side switching element 10) turns OFF a certain delay time after the HIGH level Vc signal turns on transistor 702 (fig. 1), as disclosed at col. 3, lines 57-65.

> The high level generation control signal Vc also turns on the transistor 702 of the second driving circuit. Thus, electric charge of the gate of the low-side switching element 10 is discharged through the resistor 701 and the transistor 702 to the ground, so that the low-side switching element 10 turns off a certain delay time after the generator control signal turns on the transistor 702. The delay time is set according to the resistances of the resistor 701 and a capacity of the gate of the low-side switching element 10.

We note again that Asada discloses when transistor 9 turns OFF the high-side terminal of alternator field coil 32 becomes lower than ground potential and a backflow (i.e., negative) current flows from a grounded portion through the channel and parasitic diode to the high-side terminal of field coil 32 [col. 4, lines 4-10; col. 8, lines 4-15]. We find this backflow

current flows in a negative direction, opposite to the positive direction of current flow from the positive terminal of the battery through the field coil that occurs when field coil 32 is energized by transistor 9 turning ON.

We further note, as pointed out by appellants, that when the voltage at node Vx lowers (i.e., at the instant when transistor 9 turns off power to field coil 32) the backflow (i.e., negative) current from field coil 32 initially begins to flow through parasitic diode 100 (fig. 4) to produce an initial negative voltage drop (with respect to ground) across resistor 800 at Vs (fig. 4), that triggers comparator 840 to change state and turn ON transistor 10 via the logic of NAND gate 501 and second driving circuit 7 [see brief, page 5, ¶1]. See Asada at col. 3, line 66 through col. 4, line 10:

> Thus, the second driving circuit 7 turns off the low-side switching element 10 the delay time after the battery voltage becomes lower than a regular battery voltage proportional to the reference voltage, and turns on the same a certain time after the battery voltage becomes equal to or higher than the regular battery voltage. When the low-side switching element 10 turns on, and the high-side terminal of the field coil 32 becomes lower than the ground voltage, back-flow current flows from a grounded portion through the channel and parasitic diode to the high-side terminal of the field coil 32. Accordingly, the field coil 32 is supplied from the low-side switching element 10 with the back-flow current [emphasis added].

After carefully considering all of the evidence before us, we agree with appellants that Asada fails to disclose the recited limitation of: “configuring a first circuit of the self-gated transistor to disable the transistor substantially upon a positive current flow through the transistor” [brief, page 4; reply brief, page 5; see also claim 1, emphasis added]. We do not find the

examiner's arguments persuasive regarding the comparator offset voltages and associated delays. In particular, we do not agree with the examiner's finding that the negative input terminal of the comparator must be a positive voltage (i.e., with respect to ground) in order to turn OFF transistor 841. To the contrary, we find the negative terminal of comparator 840 never attains a positive voltage potential above ground. We find that the examiner is confusing a positive voltage with respect to ground (and associated positive current flow) with a positive voltage potential occurring between comparator inputs Vs and Vr.

We note that comparator 840 changes state according to whether the voltage (Vs) at the inverting (-) input crosses above or below the reference voltage (Vr) at the non-inverting (+) input. We agree with appellants that this point will occur when both comparator input voltages are still negative (i.e., with respect to ground potential). Therefore, we agree with appellants that there is a negative current flowing through transistor 841 at the instant in time when transistors 841 and 10 are disabled when Vs becomes more positive than Vr, but where both Vs and Vr are negative voltages with respect to ground potential. We find that this point of disablement occurs when the field coil backflow current is almost fully discharged and approaching ground potential but where the negative voltage Vs dropped

across resistor 801 (fig. 5) [or resistor 800, fig. 4] becomes less negative than Vr.

We agree with appellants that the inverting (-) input to comparator 840 shown in fig. 5 (i.e., corresponding to node Vs, fig. 4) can never have a positive voltage potential (and associated positive current flow) with respect to ground potential. We note that transistor 10 is OFF (i.e., with NO current flowing through it) when field coil 32 is energized by current flowing through transistor 9 [col. 5, line 66 through col. 5, line 3]. Again, we note that when transistor 9 turns OFF, a negative backflow current flows initially through the parasitic diode to provide a negative voltage drop across resistor 801 to trigger the comparator to change state to turn ON (i.e., enable) transistors 10 and 841 that function to shunt the field coil backflow current to ground. Therefore, we agree with appellants that the negative discharge current will progressively become less negative as the field coil discharges through transistors 10 and 841 (fig. 5) until a point is reached when the voltage potential at Vs approaches ground potential (i.e., at the point of full field coil discharge). However, we note that just before this point of full discharge is reached, the comparator is triggered to change state (i.e., when Vs > Vr, but both Vs and Vr are negative with respect to ground potential), as discussed supra.

Therefore, we agree with appellants that at the instant when transistors 10 and 841 are disabled (i.e., occurring in time slightly before the field coil backflow current is fully discharged to ground), the backflow current through transistors 10 and 841 is still negative [see brief, page 5, ¶2]. We further agree with appellants that the only way to re-enable transistors 10 and 841 is by field coil 32 voltage Vx again going negative (in response to generation control signal Vc disabling (i.e., turning OFF) transistor 9 [see brief, page 5, ¶3]. Thus, we agree with appellants' conclusion that Asada discloses initially enabling (i.e., after transistor 9 turns OFF) and then disabling (after the field coil discharges) transistors 10 and 841 in response to two different values of a negative current [see brief, page 7].

Accordingly, we will reverse the examiner's anticipation rejection of representative claim 1 for essentially the same reasons argued by appellants in the briefs. Because dependent claims 2-7 contain the same limitations as independent claim 1, we will also reverse the examiner's anticipation rejection of these claims.

II. We consider next the examiner's rejection of claims 8-11 as being anticipated by Asada. Since Appellants' arguments with respect to this rejection have treated these claims as a single group which stand or fall

together, we will consider independent claim 8 as the representative claim for this rejection. See 37 C.F.R. § 41.37(c)(1)(vii)(2004).

With respect to representative claim 8, appellants argue that Asada does not disclose a method of disabling the transistor for a current flow in one direction and enabling the transistor for a current flow in the opposite direction [brief, page 7]. Appellants assert that Asada discloses disabling transistors 10 and 841 responsively to a voltage (resulting from a negative current) that is less negative than reference Vr and discloses enabling transistors 10 and 841 in response to a more negative current [id.]. Therefore, appellants conclude that Asada discloses enabling and disabling transistors 10 and 841 in response to two different values of a negative current [id.].

We note that the examiner simply restates the same arguments for claim 1 that we have addressed supra. We agree with appellants' conclusion that Asada discloses enabling and disabling transistors 10 and 841 in response to two different values of a negative current, as discussed supra [see brief, page 7]. Therefore, we will reverse the examiner's anticipation rejection of representative claim 8 for essentially the same reasons argued by appellants in the briefs. Because dependent claims 9-11 contain the same limitations as independent claim 8, we will also reverse the examiner's anticipation rejection of these claims.

III. We consider next the examiner's rejection of claims 12-18 as being anticipated by Asada. Since Appellants' arguments with respect to this rejection have treated these claims as a single group which stand or fall together, we will consider independent claim 12 as the representative claim for this rejection. See 37 C.F.R. § 41.37(c)(1)(vii)(2004).

Appellants argue that Asada does not disclose a circuit that is coupled to disable the transistor responsively to an opposite polarity of the sense signal [brief, page 8]. Appellants again assert that Asada discloses using a negative current for enabling transistors 10 and 841 and using a less negative current for disabling transistors 10 and 841 [id.]. Appellants conclude that Asada does not meet the language of claim 12 because both polarities of the current used by Asada are negative [id.].

We note that the examiner restates the same arguments for claim 1 that we have addressed supra. We agree with appellants' conclusion that Asada discloses enabling and disabling transistors 10 and 841 in response to two different values of a negative current, as discussed supra [see brief, page 7]. Therefore, we will reverse the examiner's anticipation rejection of representative claim 12 for essentially the same reasons argued by appellants in the briefs. We note that appellants have separately argued dependent claims 19 and 20 [brief, pages 9 and 10]. Because dependent

claims 13-20 each contain the same limitations as independent claim 12, we will also reverse the examiner's anticipation rejection of these claims.

Therefore, we agree with appellants that the examiner has failed to meet his/her burden of establishing a prima facie case of anticipation with respect to representative claim 1 and also with respect to independent claims 8 and 12 that recite essentially equivalent limitations.

In summary, we will not sustain the examiner's rejection of any claims under appeal. Therefore, the decision of the examiner rejecting claims 1-20 is reversed.

REVERSED

KENNETH W. HAIRSTON Administrative Patent Judge	)
JERRY SMITH Administrative Patent Judge	) BOARD OF PATENT) APPEALS AND) INTERFERENCES
ALLEN R. MACDONALD Administrative Patent Judge	)

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