The opinion in support of the decision being entered today is *not* binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte TOKUROH OZAWA

Appeal 2006-3013
Application 10/367,849
Technology Center 2600

Decided: September 19, 2007

Before JOSEPH L. DIXON, ROBERT E. NAPPI, and JOHN A. JEFFERY, *Administrative Patent Judges.*

NAPPI, *Administrative Patent Judge.*

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. §§ 134 and 6(b) of the Final Rejection of claims 14 through 24, 31, and 32; claims 25 through 30 have been indicated by the Examiner as containing allowable subject matter; and claims 1 through 13 have been canceled. We heard the appeal on September 11, 2007. For the reasons stated *infra,* we reverse the Examiner's rejection of these claims and enter a new ground of rejection.

INVENTION

The invention is directed to an active matrix display. Specifically, it relates to a layout that optimizes the display. See page 1 of Appellant's Specification. Claim 14 is representative of the invention and reproduced below:

> 14. A display apparatus comprising:
> a plurality of scanning lines;
> a plurality of data lines;
> a plurality of power-feed lines; and
> a plurality of pixels formed in a display section, the plurality of pixels being formed corresponding to intersections of the plurality of scanning lines and the plurality of data lines, each pixel of the plurality of pixels comprising a transistor and a light-emission element having a pixel electrode and a counter electrode,
> a gate electrode of the transistor being at a potential corresponding to a signal supplied from one data line of the plurality of data lines, and
> the light-emission element emitting a light when a current flows through the counter electrode, the pixel electrode, the transistor and one power-feed line of the plurality of power-feed lines,
> the line width of a portion of the power-feed line being set to be wider than that of a portion of the one data line, and
> the portion of the power-feed line and the portion of the one data line being in the display section.

REFERENCES

The references relied upon by the Examiner are:

Holmberg	US 4,820,222	Apr. 11, 1989
Kawaguchi	US 5,670,994	Sep. 23, 1997
Ota	US 5,854,616	Dec. 29, 1998
Dingwall	US 5,903,246	May 11, 1999

Hashimoto US 6,295,043 B1 Sep. 25, 2001

The additional references we rely upon are:

Johannes Adam, *New Correlations Between Electrical Current and Temperature Rise in PCB Traces*, 20th IEEE SEMI-THERM Symposium, 2004, *available at* http://www.flomerics.com/flotherm/technical_papers/t341.pdf

Web-based document *PCB Trace*, HardwareBook (HwB), *at* www.hardwarebook.info/PCB_trace (providing data tables for circuit board trace width).

REJECTIONS AT ISSUE

Claims 14, 31, and 32 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dingwall in view of Kawaguchi. The Examiner's rejection is on pages 3 and 4 of the Answer.

Claims 15, 22, and 23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dingwall in view of Kawaguchi and Ota. The Examiner's rejection is on pages 4 and 5 of the Answer.

Claim 16 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Dingwall in view of Kawaguchi, Ota and Hashimoto. The Examiner's rejection is on page 5 of the Answer.

Claims 17 through 21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dingwall in view of Kawaguchi, Ota, Holmberg and Hashimoto. The Examiner's rejection is on page 6 of the Answer.

ISSUES

Appellant contends that the Examiner's rejection under 35 U.S.C. § 103(a) is in error. Appellant argues that it is not obvious to modify Dingwall using Kawaguchi's teachings. Appellant reasons Kawaguchi involves liquid crystal devices which do not need a power feed line and that Kawaguchi teaches increasing the width of connecting terminals to reduce connection resistance and not line width within the display area as claimed. (Br. 9). Appellant argues that "Dingwall and Kawaguchi contain no teaching or suggestion of the advantages realized by a device according to claim 14." (Br. 10). Finally, Appellant argues that the Examiner's reasoning as to why one would be motivated to combine the references is based upon hindsight reasoning as the references do not provide the motivation asserted by the Examiner.

The Examiner asserts that the rejection is proper. The Examiner states that Kawaguchi was cited to show that the resistance of a power line will be reduced when the width of the power line is increased. (Answer 6). Further, the Examiner states:

> Even though Kawaguchi does not teach a line width of a portion of the one power-feed line being set to be wider than that of a portion of the one scanning line, Kawaguchi teaches the width of power feed line would be increased in order to reduce the resistance of the power feed line (see column 15, lines 24-32). There are only three width relationships between the power feed line and a data line in a display device: a) the width of power feed line is wider than a data line; b) the width of power feed line is same as a data line and c) the width of power feed line is narrower than a data line. Even though Dingwall does not point out the width relationship between the power feed line and a scanning line, Dingwall should choose the width of power feed

> line is wider than a data line lines to save more power without decrease a display area since the power supply lines(VDD) consume more power than the data lines since the power supply lines(VDD) needs to drive transistors(TR) and LEDs and the data lines(column lines) only drive transistors(T) (see Dingwall's figure 2 and Kawaguchi's column 15, lines 24-32) and this decision is generally recognized as being within in the level of ordinary skill in the art. On the other hand, there is no one or no rule to restrict that the power-feed line can not wider than a scanning line in an LED or EL display device; and Dingwall can choose any one of the above three choices.

(Answer 7). Further in the statement of the rejection the Examiner finds that modifying Dingwall would be obvious since:

> it is well known in the art that the resistance of a power supply line can be reduced by increasing the width of the power line according to the teaching of Kawaguchi et al and a formal of R=YI/A, wherein A is the cross sectional area; I is the length of the wire and Y is the resistively of the material; the width of power supply lines are wider than the data lines would be save more power without decrease a display area since the power supply lines(VDD) consume more power than the scanning lines since the power supply lines(VDD) needs to drive transistors(TR) and LEDs and the data lines(column lines) only drive transistors(T) (see Dingwall's figure 2 and Kawaguchi's column 15, lines 24-32).

(Answer 4)

Thus, the issues before us are whether:

a) the combination of Dingwall and Kawaguchi teaches or suggests a display where the power line portions on the display are wider than the data line portions as claimed;

b) the combination of Dingwall and Kawaguchi teaches or suggests the advantages realized by the device;

c) the Examiner has properly established that one skilled in the art would combine the teachings of Dingwall and Kawaguchi.

FINDINGS OF FACT

1. Dingwall teaches a circuit for driving a column of pixels in a display using organic light emitting diodes (O-LEDs). (Abstract).
2. Dingwall's circuit has scan lines (lines titled ROW_1, ROW_2, etc.), data lines (lines titled COL1, COL2, etc) and power feed lines (lines titled VDD). Fig. 2, column. 4, lines 47-56.
3. At the intersection of each of the row and column lines (claimed scan and data lines) is a pixel circuit. The pixel circuit consists of two transistors a capacitor and O-LED (e.g. pixel P1 consists, of transistor T1, TR1, C1 and an O-LED). Dingwall, Fig 2.
4. Each column (i.e. the claimed data line) also contains a reference pixel, or dummy pixel circuit. The reference pixel circuit contains a transistor and O-LED and is appended to the last pixel circuit in the column. Dingwall, Fig, 2 (items 212, PR), column 4, lines 57-60.
5. The reference pixel is used to establish the proper current for each pixel circuit in the column. The pixel circuits for the other pixels in the column mirror (via a current mirror) the current on the column line (claimed data line), i.e., the current draw from the power line by the other pixel circuits mirrors the current draw of the reference pixel circuit. Dingwall, column 4, lines 65-67, column 5, lines 11, 24.
6. The Web page (www.hardwarebook.info/PCB_trace) discusses a design rule (standard) IPC-2221 and Mil-STD-275, which identifies

how to calculate the minimum printed circuit board trace width. The Web page provides tables and graphs, and identifies for a trace thickness of 35µm, the minimum widths for different current values. P. 1 of printout.

7. Adam's article also discusses a design rule (standard) IPC-2221 and MIL-STD-275. (Abstract).
8. Adam identifies that the standards are "used as a 'design rule' for trace geometry (i.e. trace cross-section) for a given pair of current and temperature rise)." Introduction, second paragraph.
9. Adam also identifies that the resistance is dimension dependent, i.e. resistance is lower per unit length, when the trace is wider. Page 2, formula 3.
10. While we note that the Web document (discussed in fact 6) is undated, we nonetheless find that it establishes the level of skill in the art at the time of Appellant's filing of the application. Both the web document and Adam refer to the two standards IPC-2221 and MIL-STD-275 as providing the guidance for sizing trace width, and Adam identifies the standards were published in 1956 (well before Appellant's filing date). Introduction, second paragraph.
11. From Facts 6 through 10, we find that the skilled artisan would know to size (set the width of) conductive traces (lines or leads) on a printed circuit board based upon current in the trace.
12. Appellant's admitted prior art of Figure 22 teaches a display circuit with a plurality of pixels and which makes use of data, scan and

power lines. Appellant's Figure, 22, p. 3 of Appellant's originally filed Specification.

13. Each pixel circuit in the display shown in Appellant's admitted prior art contains two transistors (20 and 30) and one light emission element (item 40). The gate electrode of one of the transistors (30) is at a potential corresponding to the signal supplied on the data line. Appellant's Figure 22.
14. The load on the sig line (data line) is the capacitor and transistor (20), where as the load on the common (power line) is the capacitor, transistors (20 &30), and the light emitting element (40). Appellant's Figure 22.

PRINCIPLES OF LAW

On the issue of obviousness, the Supreme Court has recently stated that "the obviousness analysis can not be confined by a formalistic conception of the words teaching, suggestion and motivation." *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1741, 82 USPQ2d 1385, 1396 (U.S. 2007). Further, the court stated "[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1739, 82 USPQ2d 1385, 1395 (U.S. 2007).

> When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, § 103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a

> person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. . . . [A] court must ask whether the improvement is more than the predictable use of prior art elements according to their established functions.

Id. at 1740, 82 USPQ2d at 1396. "One of the ways in which a patent's subject matter can be proved obvious is by noting that there existed at the time of the invention a known problem for which there was an obvious solution encompassed by the patent's claims." *Id.* at 1742, 82 USPQ2d at 1397.

ANALYSIS

We will address the third issue first as it is dispositive of our holding to reverse the Examiner's rejection. Independent claim 14 recites a display apparatus which includes scanning, data and power lines, these lines connect to a plurality of pixel circuits that contain a transistor and light emission element. Claim 14 also recites that a portion of the power feed line, in the display section, is wider than the data line in the display section. Independent claim 31 recites similar limitations concerning the display, but instead of reciting the relative width of the data and power lines, claim 31 recites that the "resistance value per unit length of the one power-feed line being set to be smaller than that of the one data line."

The Examiner has found that it is well-known that the resistance of a power line can be reduced by increasing the width of the power line. (Answer 4). The Examiner relies upon Kawaguchi for this teaching. (Answer 4). We concur with the Appellants that the teachings of

Kawaguchi which the Examiner's rejection cites to, discuss making connection portions wider to decrease contact resistance and not making conductive lines on the display wider, as claimed. Nonetheless, we concur with the Examiner's underlying finding that it is well-known in the art that the resistance of a power supply line can be reduced by increasing the width of the power line. See for example facts 6 through 11, which discuss design rules/standards for line width on printed circuit boards. Further, we concur with the Examiner's statement that there can only be three possible relationships between the size of the power lines and the data leads, they can either be the same size, narrower or wider. In our view, a skilled artisan would choose the width of the power lead based upon the particular requirements of a given circuit arrangement (e.g., the current load on the circuit). Thus, we concur with the Examiner's finding that one skilled in the art would be motivated to size the lines on the display based upon the current load on the line.

However, we disagree with the Examiner's finding that in Dingwall's display panel, sizing the line based upon the current would result in the power line being wider than the data line. The Examiner's rationale is that the data lead (COL1) only has the load of the transistor T1, and therefore has a lower current load than the power lead which has the load of transistor TR1 and the O-LED. (Answer 4). We disagree with the Examiner's finding. The data line also has the load of the reference pixel. (Fact 4). Further, Dingwall teaches that the pixel drive circuit which is powered by the power line is a current mirror, i.e. the current mirror caused the current in the power line to mirror (be the same) as the current in the data line. (Fact

5). Based upon the current being the same in both the data and the power line, we do not conclude that one skilled in the art would make the power lines wider based upon differences in the load on the lines. Thus, we do not reach the other issues a) and b), as based upon this issue c), we will not sustain the Examiner's rejection of claims 14, 31, and 32 as unpatentable over Dingwall in view of Kawaguchi.

NEW GROUNDS OF REJECTION PURSUANT TO 37 C.F.R. § 41.50(B).

37 C.F.R. § 41.50(b) states:

> (b) Should the Board have knowledge of any grounds not involved in the appeal for rejecting any pending claim, it may include in its opinion a statement to that effect with its reasons for so holding, which statement constitutes a new ground of rejection of the claim. A new ground of rejection pursuant to this paragraph shall not be considered final for judicial review.

ANALYSIS

We now enter a new rejection of independent claims 14 and 31 under 35 U.S.C. § 103(a) based upon Appellant's admitted prior art of Figure 22 in view of the well-known sizing of power and data lines. The admitted prior art of Figure 22 teaches a display which has data and power lines. (Fact 12). This display is different than Dingwall, however, in that it does not use a current mirror. Rather, the display of Figure 22 is arranged such that the only load on the sig line (data line) is the capacitor and transistor (20), whereas the load on the common (power line) is the capacitor, transistors (20

&30), and the light emitting element (40). (Fact 14). Thus, in the display shown in Appellant's admitted prior art Figure 22, the load on the power line is greater than the load on the data line. As we indicated previously, one skilled in the art would have known to size conductive traces based upon the current load. (Fact 11). With this knowledge, we find that the skilled artisan would have made the power lines wider than the data lines, i.e., we find that the skilled artisan would have recognized that there existed a known solution of a known problem of sizing lines of a circuit board. Further, with respect to claim 31, which recites that the "resistance value per unit length of the one power-feed line being set to be smaller than that of the one data line," we find that one skilled in the art would have recognized that making the power line wider than the data line, the resistance value per unit length of the power line would be less than that of the data line. (Fact 9).

Further, Appellant's arguments that the combination of the references does not teach the advantages of the claimed invention is of no consequence to our new rejection as independent claims do not recite limitations drawn to the advantages argued by Appellant on page 10 of the Brief. Accordingly, we now reject independent claims 14 and 31. We leave it to the Examiner to determine if rejections based upon similar rationale apply to the remainder of the pending claims.

CONCLUSION

Appellant's contentions have convinced us of error in the Examiner's rejection of claims 14, 31, and 32 under 35 U.S.C. § 103(a), and we reverse

this rejection. The Examiner has not shown that the additional references relied upon to reject claims 15 through 24 make up for the deficiencies noted in the rejection of independent claim 14. Accordingly, we also reverse the Examiner's rejection of claims 15 through 24 under 35 U.S.C. § 103(a). In accordance with 37 C.F.R. § 41.50(b) we also now reject independent claims 14, and 31 under 35 U.S.C. § 103(a) as being obvious.

ORDER

The decision of the Examiner is reversed.

This decision contains a new ground of rejection pursuant to 37 C.F.R. § 41.50(b) (effective September 13, 2004, 69 Fed. Reg. 49,960 (August 12, 2004), 1286 Off. Gaz. Pat. Office 21 (September 7, 2004)). 37 C.F.R. § 41.50(b) provides "[a] new ground of rejection pursuant to this paragraph shall not be considered final for judicial review."

37 C.F.R. § 41.50(b) also provides that the Appellant, WITHIN TWO MONTHS FROM THE DATE OF THE DECISION, must exercise one of the following two options with respect to the new ground of rejection to avoid termination of the appeal as to the rejected claims:

> (1) *Reopen prosecution*. Submit an appropriate amendment of the claims so rejected or new evidence relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the proceeding will be remanded to the examiner. . . .
>
> (2) *Request rehearing*. Request that the proceeding be reheard under § 41.52 by the Board upon the same record. . . .

REVERSED - 37 C.F.R. § 41.50(b)

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Add A Page | Delete Last Page

Notice of References Cited	Application/Control No. 10/367,849	Applicant(s)/Patent Under Reexamination	
	Examiner Lun-Yi Lao	Art Unit 2600	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification	
	A	US-			--	--
	B	US-				
	C	US-				
	D	US-				
	E	US-				
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FOREIGN PATENT DOCUMENTS

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	N						
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	P						
	Q						
	R						
	S						
	T						

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
*	U	Johannes Adam, New Correlations Between Electrical Current and Temperature Rise in PCB Traces, 20th IEEE SEMI-THERM Symposium, 2004, available at http:www.flomerics.com/flotherm/technical_papers/t341.pds
*	V	Web-based document PCB Trace, HardwareBook (HwB), at www.hardwarebook.info/PCB_trace (providing data tables for circuit board trace width)
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

New Correlations Between Electrical Current and Temperature Rise in PCB Traces

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Abstract

The widely used design rule IPC-2221 (=MIL-STD-275) for the 'current carrying capacity' of traces on printed circuit boards is subject of a closer investigation. These historical studies on correlations between electrical current and temperature rise of the trace can be reproduced by numerical heat transfer simulations only if the board has a back 35µm copper layer and the thickness of the trace is 35 µm. As this makes an extrapolation to other boards impossible, we will present numerical studies for FR4-based board models with other copper planes and also for ceramic substrates. For a better understanding of the results, 2D heat conduction calculations for traces on boards with constant internal and external conditions are performed. Quantitatively, they can be interpreted as parallel thermal resistances of the trace and the rest of the board, where we treat the board approximately as a heat sink fin. These semi-analytic limits give scaling laws for the thermal resistance of the trace as function of board conductivity, heat exchange coefficient, board thickness and trace width. For the more realistic board models this simplified theory is not powerful enough as the thermal isolation between trace and first copper plane is not included.

Keywords

Joule heating, current, PCB cooling, CFD

1. Introduction

An electrical current flowing in a copper wire causes deposition of thermal energy in that wire. To honour James Joule [1], the discoverer of the effect, it is called "Joule heating". Joule heating also plays an eminent role for copper traces on printed circuit boards (PCBs). The temperature of a copper trace on a PCB is the result of thermal equilibrium between Joule *heating* and convective and radiative *cooling* by the heat flux from the board to the ambient environment. However, there are technological limitations to the temperature of a copper trace: the temperature of the trace must not exceed certain limits, e.g. the glass transition temperature of FR4 around 110 degC or a comparable limit due to solder stability aspects. Joule heated traces on PCBs are the 'energy pipelines' in automotive control units and other power control devices.

In recent years the electrical power consumption in automobiles rose and hence a reasonable prediction of trace and board temperatures is needed. For this purpose, the graphs in IPC-2221 (=MIL-STD-275) are widely used as a 'design rule' for trace geometry (i.e. trace cross-section) for a given pair of current and temperature rise. They had been published by the National Bureau of Standards back in 1956. There are well-founded doubts whether this 'standard' is really useful and valid. First, layout experts tell, that usually higher currents can be put on a trace. Second, the IPC2221 diagrams for so-called internal conductors (those inside the PCB) are de-rated in current by a factor of exactly two with respect to external conductors (those on the surface of the PCB). These suspicious facts make it necessary to ask for further theoretical and experimental investigations. There is also need for new correlations because new materials and geometries have emerged since the fifties.

2. The IPC-2221 design rule

2.1. The data

The design rule IPC-2221 (=IPC-D-275=MIL-STD-275) (Fig.1) is widely used to estimate the temperature rise due to an electrical current. The usage is according to the following two steps (dashed lines)):

Step 1: determine the cross-section A of the trace (in square mils) in the lower diagram from trace width (in inches) and the thickness (in ounces of copper per square foot, 1 oz is about 35 µm, 2oz=70 µm).

Step 2: Transform the cross-section to the upper diagram and read the data couple of current I and temperature rise ΔT.

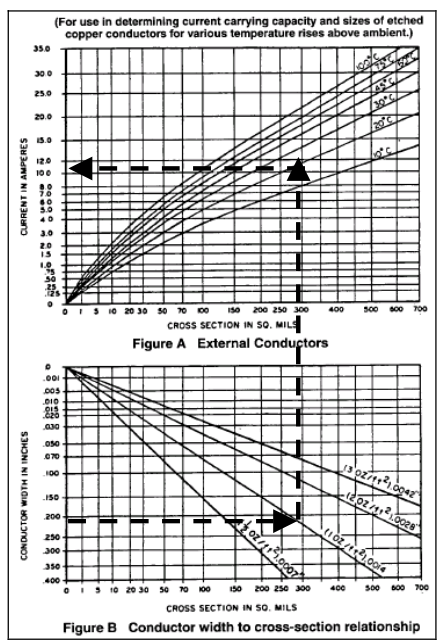


Figure 1: Nomograph from IPC-2221 for „external conductors" [2] with example of usage.

2.2. Origin and reproducibility

While working on a revision of the design rule, called IPC-2152, the IPC Task Group 1-10b lead by Jouppi, found the roots of IPC-2221 as having been experimental work for

the National Bureau of Standards (NBS) back in 1956 [3,4 and references therein]. The original plots of the current vs. cross-section diagrams reproduced in [4] show a wide scatter of data points. This is due to a variety of printed boards with different structure and coating. The nomographs (i.e. Figure 1) represent the upper limit of the points. The lower limit is in close agreement with the so-called Design-News ("DN") correlations brought to our notice by Brooks [2]. Brooks also gives the following fits:

the IPC-Data (A in sq.mils) $I = 0.065 * \Delta T^{0.43} * A^{0.68}$, (1)

the DN-Data $I = 0.040 * \Delta T^{0.45} * A^{0.69}$. (2)

The pertinent questions are now: is it possible to reproduce the experimental curves by theoretical calculations? What can be learned? Can they be extrapolated to other scenarios?

To answer the first question, we perform numerical studies on a simple 3D model of a board and a trace with a commercially available code [5]. The equations which are solved in a discretized form are Fourier's equation (heat conduction), the Navier-Stokes equation together with the conservation of mass (fluid dynamics), the Stefan-Boltzmann law of radiation and some wall functions for momentum and heat transfer. We restrict our investigations on the steady-state, discrete current and laminar natural convection. Without knowledge of the exact NBS experimental arrangement, we are assuming a model with a PCB in Euro-Format (L_x=100 mm, L_y=160 mm, D=1.6 mm) made of pure FR4 (conductivity k=0.3 W/m-K, emissivity ε=0.9), with one copper trace of length L=100 mm and thickness t=35 µm (=1 oz) on the top face and with an optional copper layer on the back plane (also of thickness 35 µm, conductivity k=395 W/m-K and with a solder resist with emissivity ε=0.9) (Fig. 2).

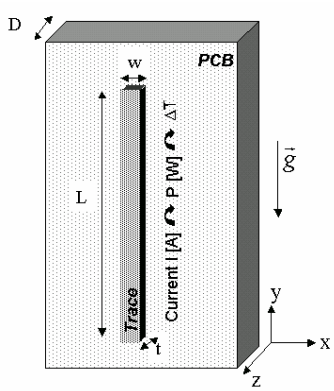


Figure 2: Description of variables of our numerical models.

The trace is characterized by a local temperature T [deg C] and geometry-dependent electrical resistance R_{el} [Ohm]

$$R_{el} = \frac{L \cdot \rho_{20}(1 + \alpha_{20}(T - T_{20}))}{t \cdot w} \quad . \qquad (3)$$

The power deposition P [W] due to current I [A] is according to Joule's law

$$P = R_{el} \cdot I^2 \quad . \qquad (4)$$

ρ_{20}=0.0175 Ohm mm²/m is the specific electrical resistivity of a copper wire of length 1 metre and cross-section 1 mm² at T_{20}=20 degC (for Eq. (3), t and w have to be in mm, L in m). The electrical resistance increases with temperature approximately at a rate of α_{20}=0.00395 K^{-1}. The cross-section of the trace is $A = t \cdot w$. The CFD calculations solve consistently the steady-state thermal equilibrium due to Joule heating and cooling by conduction, convection and radiation together with the natural convection flow field around the board. Adjusting of any parameter is neither done nor required. The results for an ambient temperature of T_a=20 degC, a mean temperature rise of the trace of ΔT=20 degC (i.e. T=40 degC) and a trace thickness of t=35 µm are compared in Fig. 3. The dashed lines are from equations (1) and (2), resp., the solid lines are results of our simulations. The trace length L is of minor importance, as both power and cooling area to the left and right increase with L.

Our calculations (Fig. 3) show that we can reproduce the *Design-News* correlation (Eq. 2) by a *bare epoxy board* with one heated trace on it, and the *IPC-2221* correlation (Eq. 1) by a board with a *backward 35µm copper plane*. Taking into account the uncertainties in both methods, the results are in reasonable agreement. The reason for the difference between IPC and DN correlations is of course the different kinds of heat spreading in the PCB. The board with 35µ copper back layer is a better heat spreader than the pure FR4 board and therefore cooler, or, can carry a higher current, respectively.

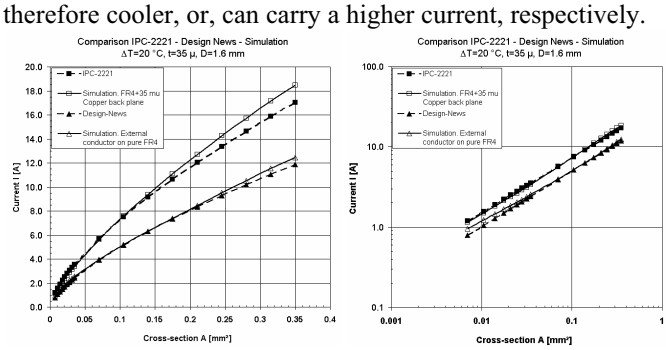


Figure 3: Simulation results (solid lines) compared with Eqs. (1) and (2) (dashed lines) on linear and log scales.

2.3. Criticism of IPC-2221

1. The close agreement between the numerical result and the IPC correlation implies that the applicability of the IPC correlations is limited to PCBs with little copper content. Nowadays PCBs contain more copper, so that they can carry more current, which is observed in practice.

2. Other calculations [6] also show that the 50% current de-rating of internal traces found in IPC-2221 is not justified but must have been a matter of speculation at that time. Internal conductors heat and cool almost like external conductors (according to our calculations current de-rating is about 5%)

3. The simple dependence on trace cross-section A cannot be correct. Consider two traces of same cross-section, but different width w and thickness t (Fig.4). Assume the traces have the same current, the heat spreading topology and hence cooling will be different. The heat flow into the PCB is primarily dominated by the footprint of the trace, i.e. by the width. The horizontal trace (left) will provide better cooling

than the vertical trace (right) and will carry a higher thermal power or electrical current for the same temperature rise.

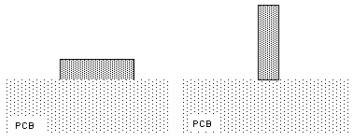


Figure 4: Flaw in IPC-2221: the two traces have the same cross-section, but they cannot have the same temperature with the same current. For the same current, the left trace must be cooler.

2.4. Validating the simulation with IPC-2152

For a revision of IPC-2221, the IPC task group 1-10b performed new experiments on current-temperature correlations. These new results [3,4] are also well reproduced by our numerical models. Board parameters, materials and environmental conditions are as described in Sect. 2.1. The IPC-2152 design rule is not yet published in its final release.

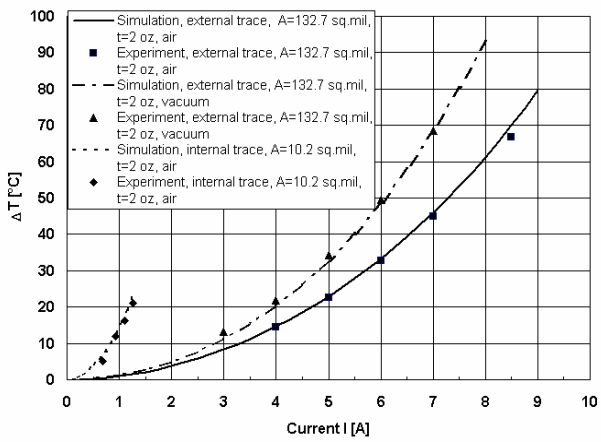
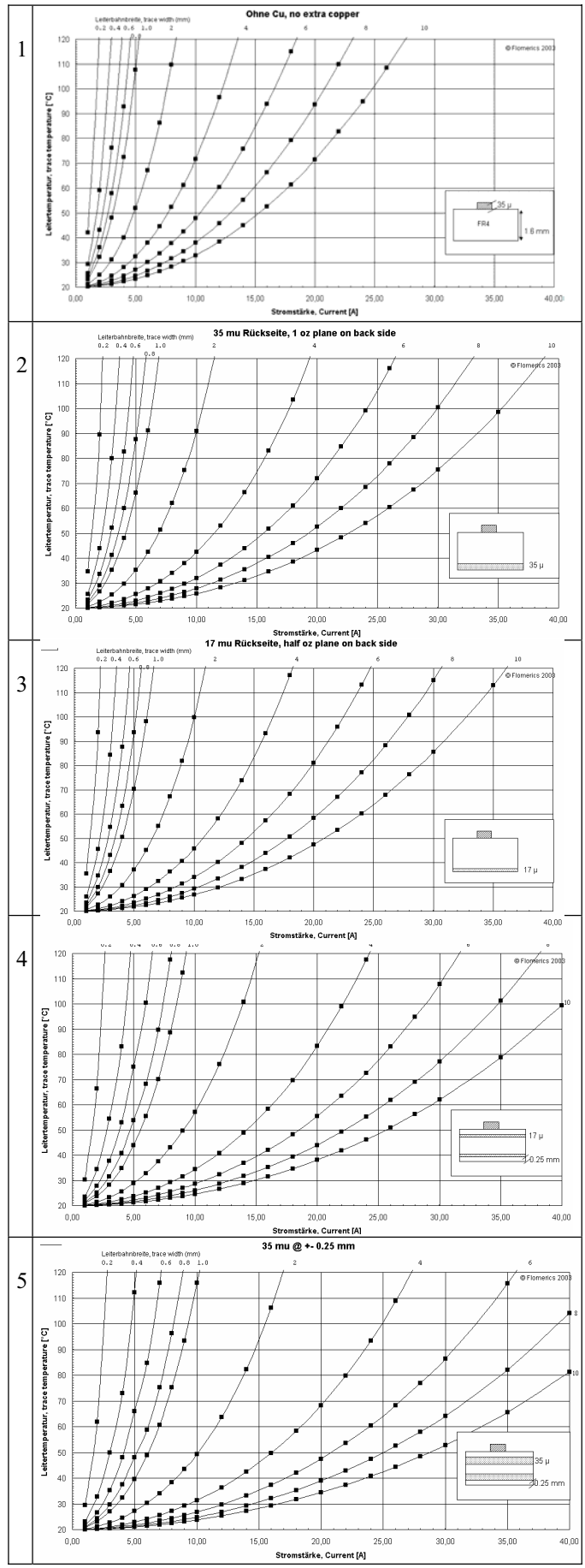


Figure 5: Simulation results compared with some new experimental data from [3].

3. New *T* vs. *I* correlations

3.1. FR4-based PCBs

The successful reproduction of the old IPC- and DN-Data and the new experiments encourages us to calculate $T(I)$ diagrams for other PCB scenarios. The base material is FR4 (k=0.3 W/m-K), board thickness is D=1.6 mm, trace thickness is t=35 µm (copper with solder resist). The copper layers extend over the PCB completely. Ambient condition is 'still air' (i.e. free convection) with T_a=20 degC. The thickness and position of additional copper layers is indicated in the insert of the diagrams and is motivated by typical application requirements to PCB manufacturers [7]. The parameter of the curves is the trace width w (in mm). The copper planes in scenarios 4-7 are symmetric with respect to the mid-plane. The temperature of the trace on the vertical axis is the calculated average temperature in the volume of the trace. There are little deviations from uniformity, which shall not be discussed here.



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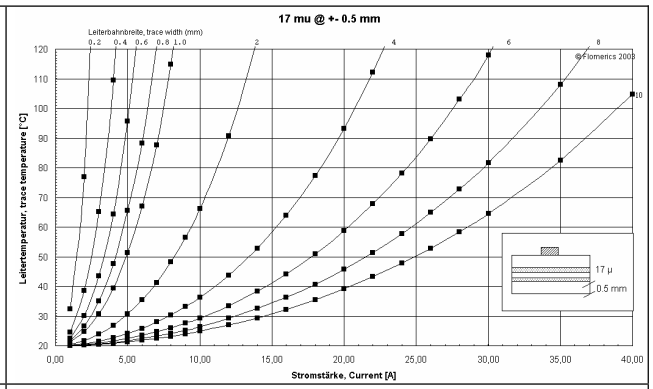

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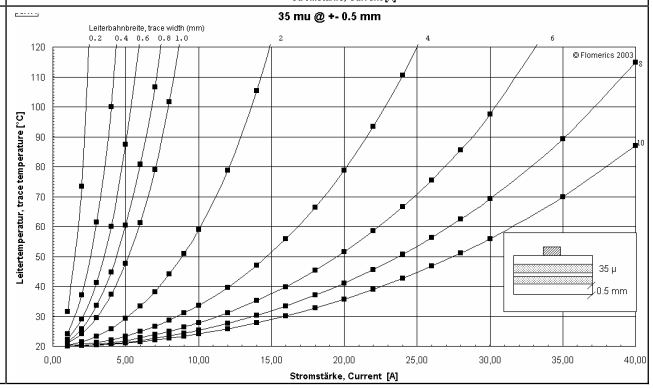

(Continued from previous page)

Table 1: Mean temperature of a trace (in 20 degC ambient) as function of electrical current for different PCB scenarios. Base material of the board is FR4. Parameter is trace width from 0.2 mm to 10 mm

It is clearly seen, that the more copper the board contains, the lower is the trace temperature, or, the higher the allowed current. If we take a look at scenarios 2,4 and 6, which have the same copper content, we see also that the thermal resistance from the trace to the plane (i.e. the distance) influences the temperature. To make comparison more clearly, the current values of some designs for a t=35 µm trace of width of 2 mm and 10 mm and temperature rise ΔT=20 K are given in Table 2.

Scenario	Current $I(\Delta T$=20 K) w=2 mm	Current $I(\Delta T$=20 K) w=10 mm
1	4.0 A	12.6 A
2	5.7 A	18.7 A
3	5.5 A	17.0 A
4	7.4 A	21.0 A
5	8.4 A	23.6 A
6	7.0 A	20.2 A
7	7.2 A	22.6 A

Table 2: Calculated current I leading to a mean temperature rise of ΔT=20 K for trace widths w=2 mm and 10 mm for different board designs.

3.2. Traces on ceramics substrate

We repeat the calculations for traces on typical ceramics material (Al_2O_3) (thermal conductivity k=16 W/m-K) and thickness D=1 mm and 0.5 mm.

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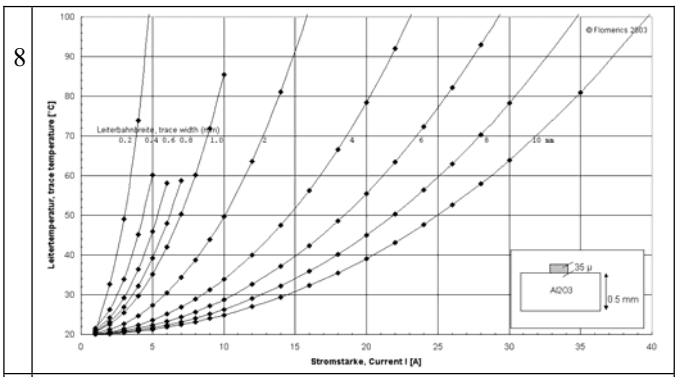

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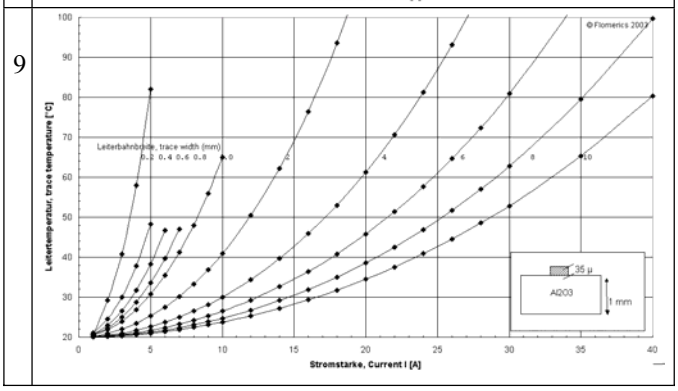


Table 3: Mean temperature of a trace (in 20 degC ambient) as function of electrical current for traces on ceramics substrate. Parameter is trace width from 0.2 mm to 10 mm.

Scenario	Current $I(\Delta T$=20 K) w=2 mm	Current $I(\Delta T$=20 K) w=10 mm
8	8.2 A	20.5 A
9	9.8 A	23.5 A

Table 4: Calculated current I leading to a mean temperature rise of ΔT=20 K for trace widths w=2 mm and 10 mm on ceramic PCBs.

Traces on polyimide film

Finally, we show the results for traces on a thin (D=0.3 mm) substrate, e.g. a polyimide film (k=0.3 W/m-K). Although this is not an exact representation of a flex-circuit, these calculations show that the thinner the substrate, the lower is the current-carrying capacity.

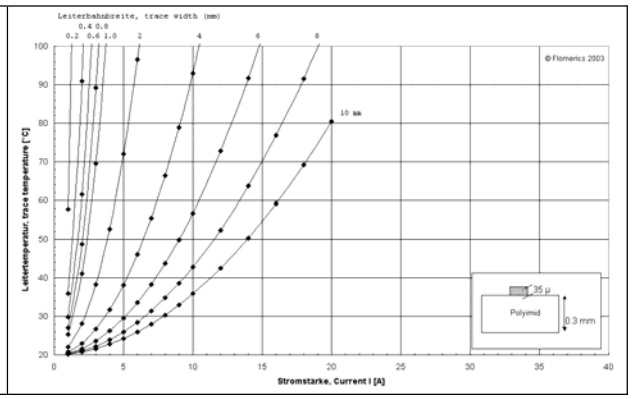
10	

Table 5: Mean Temperature of a trace (in 20 degC ambient) as function of electrical current for traces on a thin polyimide foil. Parameter is trace width from 0.2 mm to 10 mm.

3.3. Trace thickness other than 35 µm

The calculated diagrams above (as well as we believe it to be the case for those in IPC-2221) are valid for a trace thickness t=35 µm only. For a given PCB structure, the temperature of the trace is determined by the power and the footprint of the trace. If we double the thickness and increase the current by √2, we deposit the same power (see Eqs. 3 and 4) and obtain the same temperature rise, provided the *trace width w remains the same*. This scaling law for trace thickness t other than 35 µm can be written as

$$\frac{1}{35\mu\text{m}\cdot w}\cdot I_{35\mu\text{m}}^2 = \frac{1}{t\cdot w} I^2 \,. \qquad (5)$$

The l.h.s. is known data from the diagram, the r.h.s. is the desired combination of t (in µm) and I. Of course, t has to be reasonably small, so that the trace can be considered as thin trace. We have verified Eq. (5) by numerical simulations.

4. Interpretation of the results and scaling laws

4.1. Trace heating with constant properties

The style of the diagrams in Tables 1,3 and 5 was chosen as to hand over them to layouters in an easy-to-use form. From a thermal analysis point of view they should be plotted in a different way. First, the almost parabolic shape is likely to reflect Joule's $P=R_{el}\cdot I^2$ law, so we need to change over to the power, to see deviations from the parabola. Second, temperature can be included by plotting the thermal resistance R (in K/W)

$$R=\Delta T/P \qquad (6)$$

on the vertical axis (ordinate). Third, trace width as parameter should appear as independent variable on the horizontal axis (abscissa). Fourth, the conducting properties of the board/substrate should be the independent parameter.

To identify the scaling laws for a trace-like heated plate, we prepare a simplified numerical computational test environment which is free of temperature dependent cooling and heating effects. We apply a homogenously distributed fixed power in the trace (L=100 mm), allow for heat conduction only and define a cooling heat flux by Newton's law with a fixed heat exchange coefficient h=10 W/m²K on the surfaces. The board has a square shape (L=100 mm, B=100 mm, D=1.6 mm), so that we have a 2D situation (Fig. 6).

The thermal resistance R of the trace based on the mean trace temperature T, ambient temperature T_a and the power input shall be

$$R=(T-T_a)/P \quad . \qquad (7)$$

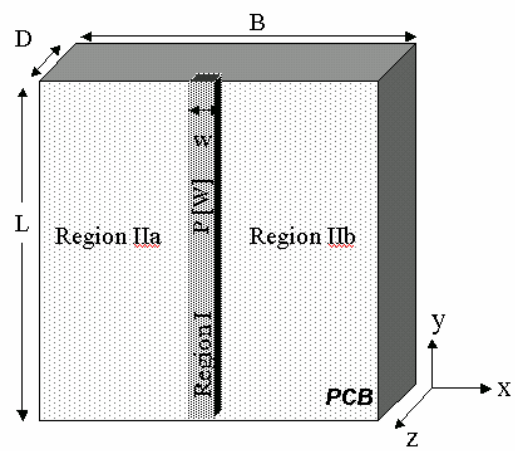


Figure 6: 2D-like test geometry with constant properties.

Fig. 7 is showing the dependence of R as function of trace width w. The trace is always centred with respect to the board. At w=100 mm, the trace is of same width as the board. The plate is either orthotropical or isotropical conducting with values indicated in the graph and notation of directions as in Fig. 6. The data points in Fig. 7 are independent of power input P.

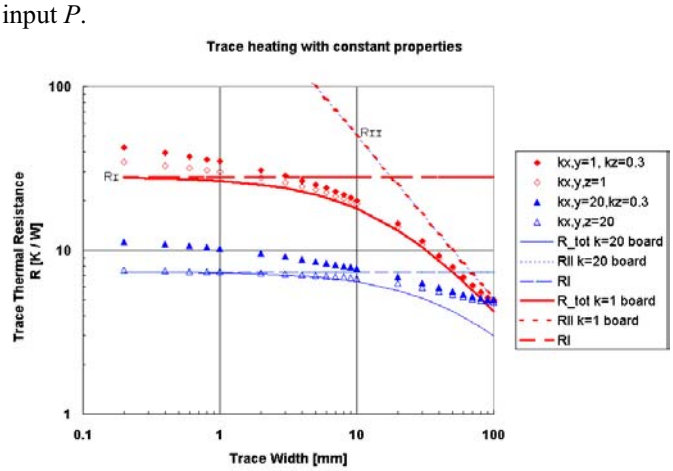


Figure 7: Numerical results for 2 pairs of constant board properties, compared with semi-analytical equations.

For a better understanding of the results of Fig. 7, we adopt a procedure from Guenin [8]. The plate is divided into 2 regions: the trace (Region I) and the board around it (Region II). For Region I, we assume Newton's cooling law for the heat flux from the footprint of the trace. For Regions IIa and IIb we interpret the physical situation as cooling of the trace by a heat sink fin. We should consider it as first-order estimate.

1. Fine trace limit

The heat flux from the trace is spread (in x-direction) by the board and the board will do the bulk of the total heat transfer. The classical heat sink fin formula [9] for a homogenously heated thin fin with (cf. Fig. 6) fin height $B/2$, fin length L and fin thickness D applied to Regions IIa and IIb is giving as thermal resistance

$$R_{\mathrm{II}} = \frac{1}{2}\frac{1}{kmDL}\frac{1}{\tanh(m\frac{B}{2})} \tag{8a}$$

with

$$m = \sqrt{\frac{2h}{kD}} \quad . \tag{8b}$$

The first factor 1/2 in Eq. (8a) is because the resistances of Regions IIa and IIb are parallel.

1. Broad trace limit

For broad traces, which cover most of the board, Region I is dominating. The thermal resistance is given by the area of the footprint and the heat exchange coefficient according to Newton's cooling law

$$R_{\mathrm{I}} = \frac{1}{2}\frac{1}{hwL} \quad . \tag{9}$$

The factor 1/2 is because the resistances of the trace on top face and the thermal image of the footprint at the bottom face are parallel.

2. The *total thermal resistance* finally is (approximately)

$$\frac{1}{R_{tot}} = \frac{1}{R_{\mathrm{I}}} + \frac{1}{R_{\mathrm{II}}} \quad . \tag{10}$$

Equations (8a,b), (9) and (10) are plotted as lines into Fig. 7 for the parameters given in the legend. The agreement is well regarding the crude mathematical modelling. The deviations between the points and the lines are of the order of √2, reflecting uncertainties in defining fin cross-section and fin surface area for Eqs. (8a) and (8b): Assuming, that only the top face of a bad heat spreading board will dominantly heat and cool, then R_{II} would be about √2 times larger.

4.2. Scaling laws

Strict analytic solutions, although with necessary simplifications, of the 2D heat conduction equation in form of Fourier series are given by Ling [10]. However, the dependence of $\Delta T(I)$ on h, k, D and w is hidden behind complicated equations. Our simplified approach is a much easier route.

1. Fine trace limit

For fine traces where Region II is dominating (note R_{II} is independent of w), the thermal resistance of the trace is

$$R_{tot} \propto h^{-1/2}k^{-1/2}D^{-1/2} \quad . \tag{11}$$

If we introduce Eq. (1) into $\Delta T = R_{\mathrm{tot}} * P$ together with Eq. (3) and (4), the desired scaling laws are simply

$$\Delta T \propto h^{-1/2}k^{-1/2}D^{-1/2}w^{-1}t^{-1}I^2 \tag{12}$$

or

$$I \propto h^{1/4}k^{1/4}D^{1/4}w^{1/2}t^{1/2}\Delta T^{1/2} \, . \tag{13}$$

2. Broad trace limit

For broad traces on low conductivity boards, Region I is dominating (note R_{I} is independent of k)

$$R_{tot} \propto h^{-1}w^{-1} \quad , \tag{14}$$

$$\Delta T \propto h^{-1}w^{-1}w^{-1}t^{-1}I^2 \propto h^{-1}w^{-2}t^{-1}I^2 \quad , \tag{15}$$

$$I \propto h^{1/2}w^{+1}t^{1/2}\Delta T^{1/2} \quad . \tag{16}$$

For high conductivity boards the width of the board B should replace w in Eq. (14) with the corresponding consequences of proportionalities in I and ΔT.

To verify Eq. (10), disregarding form factors, we perform some more parameter variations, as shown in Fig. 8. Within a factor of √2 the fine trace limit and the broad trace limit is fulfilled.

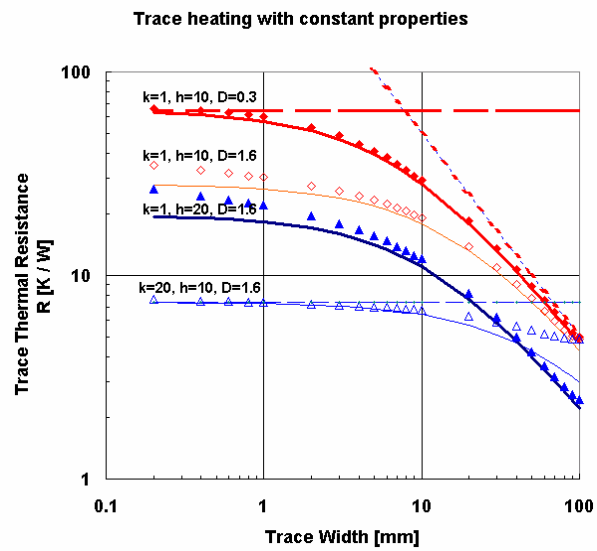


Figure 8: Testing the scaling laws by parameter variations.

4.3. Thermal resistance of the traces on board models

The board models of Sect. 4.1 are not as homogeneous as they are in Sect. 4.2 but have some thermal isolation between trace and first heat spreading copper layer. Moreover, Joule heating and external heat transfer is not independent of temperature or power. In order to test the findings of Section 4.1 we have re-plotted in Fig. 9 some graphs from Table 1, but with ordinate $R_{\mathrm{trace}} = \Delta T/P$ as function of trace width. The power P is taken from Eqs. (3) and (4) with T as the mean trace temperature.

In Fig. 9 there are two observations to be made. First, there is a bigger scatter in the data and, second, boards 2,4,6, which have the same amount of copper, are shifted in ordinate. The scatter is certainly partially due to the non-constant heat transfer, e.g., at the left end of the abscissa at w=10 mm, the lower values of R correspond to the high currents (high temperatures). In Appendix A we derive some approximate effective heat transfer coefficient h_{eff} as function of power density q related through the expression $h_{\mathrm{eff}} = 9\, q^{0.14}$. According to Eq. (11), the thermal resistance should scale with $h^{-1/2}$, namely as $q^{-0.07}$, namely as $P^{-0.07}$.

In Fig. 10 we are therefore modifying the ordinate of Fig. 9 by a multiplier $\{P(w=0.2\text{ mm};\ I=1\text{ A})/P(w;I)\}^{-0.07}$, each being a constant for the board model. Experiments with the exponent exhibit that for the pure FR4 model a value around -0.07 gives the best correlation coefficient indeed. The data points for the isotropic board model 1 are closer together now, and the trend is very similar to the low conductivity board from Fig. 7. For the other models the scatter cannot be removed. We suspect that the already mentioned temperature dependent influences and the 3D structure of the boards are beyond the capacity of the simple theory presented in Sect. 4.1. For example boards 2,4,6 have the same copper content, but significantly different thermal resistances of the trace. A posteriori, this justifies our initial numerical approach and rules out oversimplified usage of Eqs. (3), (4) and their extrapolation to other scenarios. One should always bare in mind, that for a trace thickness t other than 35 µm, Eq. (5) is still valid.

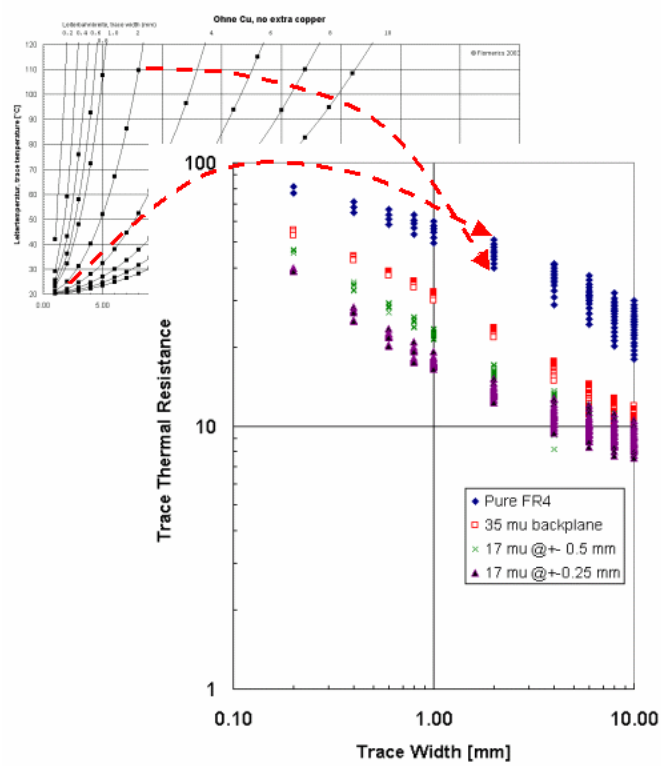


Figure 9: Uncorrected numerical thermal resistance of the trace in scenarios 1 (□), 2 (9), 4 (x) and 6 (□) from Table 1.

5. Conclusions

The aim of this article is twofold: first, we want to reproduce the graphs in design rule IPC-2221 by numerical model calculations and to review it critically, second, we want to calculate current-temperature correlations for more up-to-date board scenarios.

- As for the graphs in IPC-2221, we find that electrical engineers should be warned against regarding the graphs as being universal, and taught that its usage is restricted to certain board and trace geometries: a board with 35µm copper layer on the back and a long trace of thickness 35µm. The simple dependence of trace temperature on trace cross-section is not correct. With Eq. (5) we give a transformation law for other values of trace thickness.

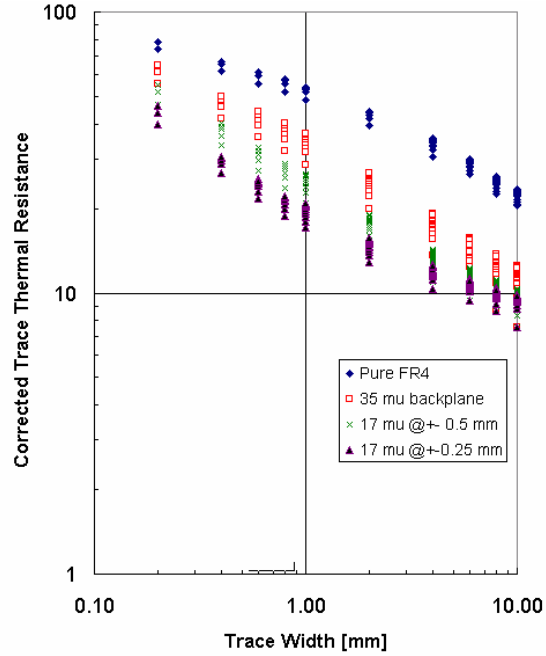


Figure 10: Re-scaled thermal resistance of the trace in scenarios 1 (□), 2 (9), 4 (x) and 6 (□) from Table 1.

- We also test our numerical model successfully against new experimental results which were undertaken for a revision of IPC-2221, called IPC-2152.
- For more up-to-date 3D board structures, we calculate new graphs for trace temperature rise as function of electrical current and trace width. The better the heat spreading, the lower of course the temperature, and the higher the allowable electrical current. Not only the copper content in the board influences the temperature but also the isolation distance between trace and first copper layer. To understand the underlying dependencies on board parameters like conductivity, thickness and heat exchange coefficient, we adopt a simple semi-analytic heat transfer model: the trace is cooling like a plate and the board around is cooling like a heat sink fin. Although being far from an analytic 2D solution, Eqs. (11) and (14) are the principle scaling laws for the thermal resistance of a trace under conditions of constant material and heat exchange properties.
- The numerical results for non-homogeneous boards and temperature dependent heating and cooling properties are not easily put into an analytical framework. The fact that boards with same copper content but different vertical position of layers have significantly different cooling characteristics justify our initial numerical (CFD-) approach.

Subject of future work are calculations with forced convection cooling, metal core or metal laminated PCBs, PCBs inside enclosures multiple heat sources and much more. Some analytical work has already been done [10] and some numerical activities have already been started [11]. Another

open field is self-consistently solving the 2- or 3-dimenisonal current distribution, i.e. power distribution, on non-straight broad traces together with the temperature field.

Acknowledgments

I gratefully acknowledge stimulating contributions from the FED (German designer association) internet discussion forum and Drs. Poschmann (FED) and Lehnberger (Andus GmbH) for valuable hints.

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Appendix. Effective heat transfer coefficient for a plate

The total heat flux balance for a homogeneously heated plate of area A is

thermal gain – convective loss - radiative loss = 0. (A-1)

With the input heat flux (thermal power) P and other standard notations [9] we have to solve the implicit equation

$$P - A \cdot h \cdot (T_{\text{plate}} - T_{\text{a}}) - A \cdot \varepsilon \cdot \sigma \cdot (T_{\text{plate}}^4 - T_{\text{a}}^4) = 0 \qquad \text{(A-2)}$$

for the plate temperature T_{plate}. We restrict ourselves to laminar, free convection. For $h(T)=\text{Nu}_\text{H}*\lambda_{\text{air}}/H$ we are using the Nusselt-Grashof correlation $\text{Nu}_\text{H}=0.49\text{Gr}_\text{H}^{1/4}$ based on the height H of the plate. For the emissivity we take ε=0.9 and for the ambient temperature T_a=35 degC. Because of the non-linear terms, the temperature of the plate T_{plate} in ambient temperature T_a has to be solved numerically (e.g. Newton-Raphson method). Eq. (A-2) can be divided by A and solved for plate temperature as function of specific heat load $q:=P/A$ [W/m²]. Fig. A-1 represents the numerical result for various board heights showing an almost perfect power law and little deviation from each other. A good numerical fit is represented by

$$\Delta T = 0.11\, q^{0.86}. \qquad \text{(A-3)}$$

The effective heat transfer coefficient h_{eff} for the plate is $h_{\text{eff}}=P/(A*\Delta T)=q/\Delta T$. Substituting for ΔT from Eq. (A-3) gives the effective heat transfer coefficient as

$$h_{\text{eff}}=9\, q^{0.14}\,. \qquad \text{(A-4)}$$

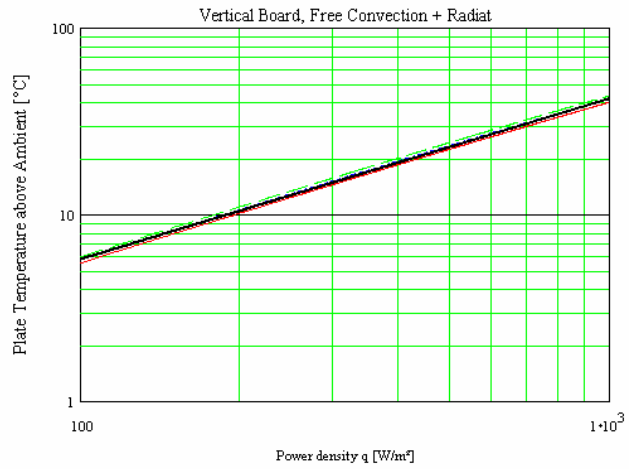


Fig. A-1: Mean temperature rise above ambient for a homogeneously heated plate in free convection and radiative cooling calculated from standard Nu-Gr heat transfer correlations (the various lines are for various board formats, e.g. Euro, double Euro and some others).

PCB trace

From HwB

According to recommendations in IPC-2221 (formerly IPC-D-275, MIL-STD-275) on how to calculate minimum PCB (printer circuit board) trace width.

Below table is valid for:

- PCB material FR-4
  - Board thickness=1.6mm (0.063")
  - Trace thickness=35µm (1 oz)
- Allowed temperature rise=10 °C

Contents

- 1 Table
- 2 Graph
  - 2.1 Outer traces (0-1 A)
  - 2.2 Outer traces (1-10 A)
  - 2.3 Inner traces (0-1 A)
  - 2.4 Inner traces (1-10 A)
- 3 Formula
- 4 Links

Table

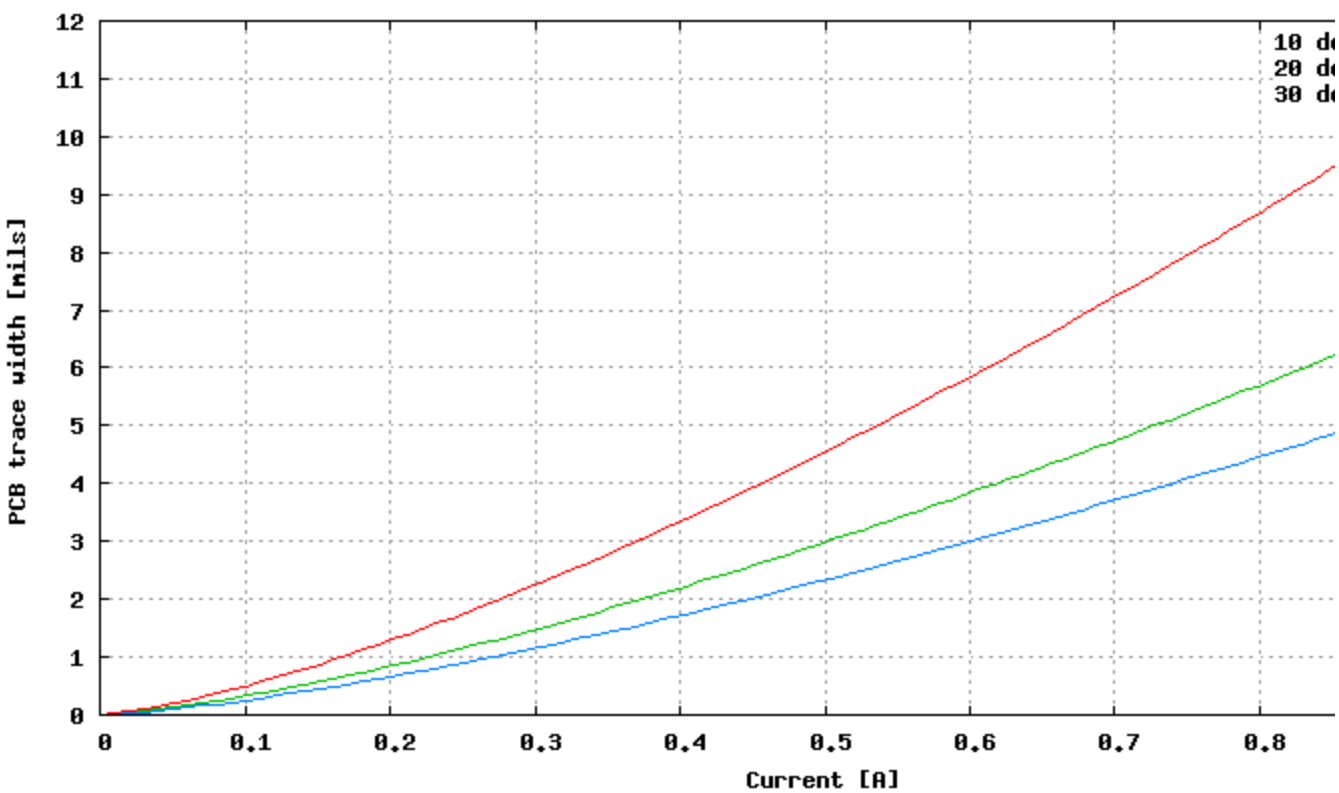
Current	Width (inner)	Width (outer)
A	mils	mils
0.01	0.308	0.118
0.05	1.54	0.591
0.1	3.08	1.18

0.2	6.15	2.37
0.4	12.3	4.73
0.4	12.3	4.73
0.5	15.4	5.91
0.6	18.5	7.1
0.7	21.5	8.28
0.8	24.6	9.46
0.9	27.7	10.6
1.0	30.8	11.8

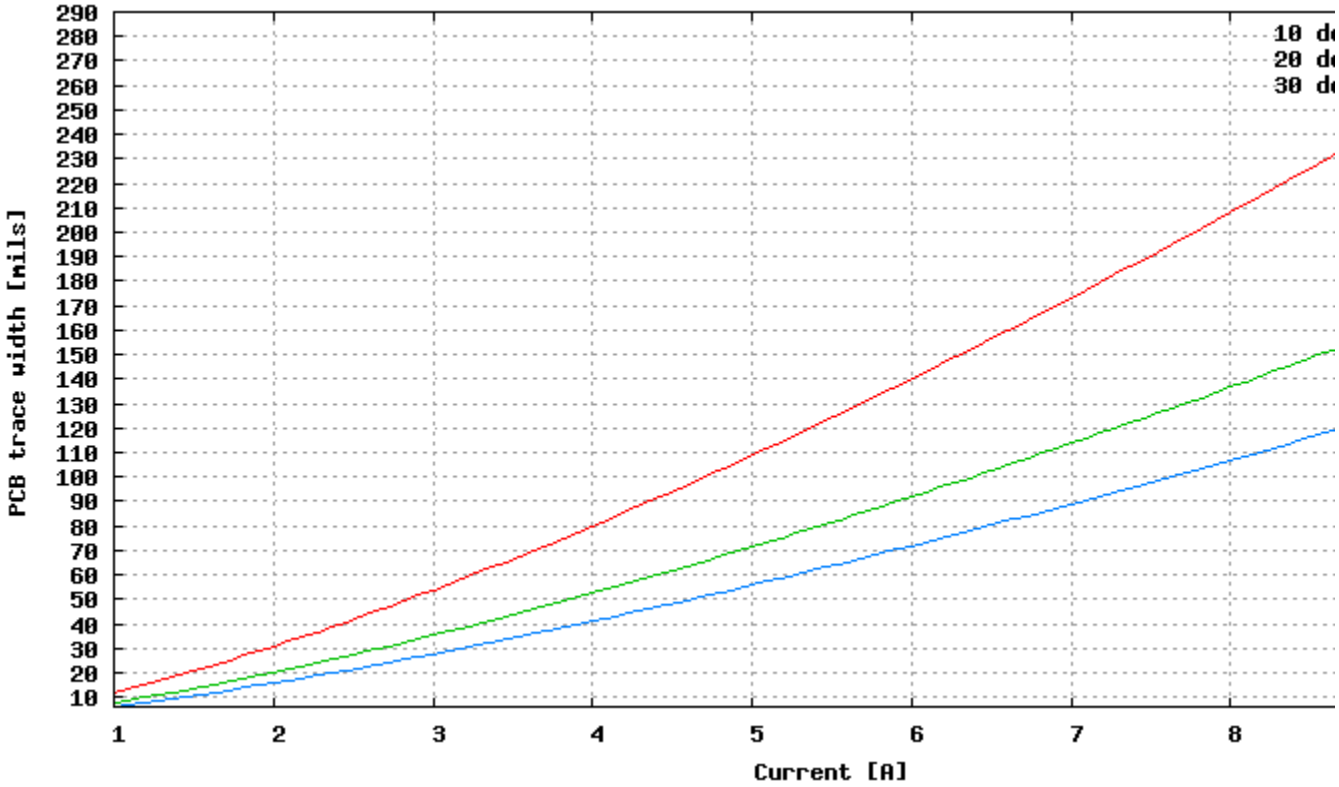
Note: 1 mil = 1/1000" = 0.0254 mm

Graph

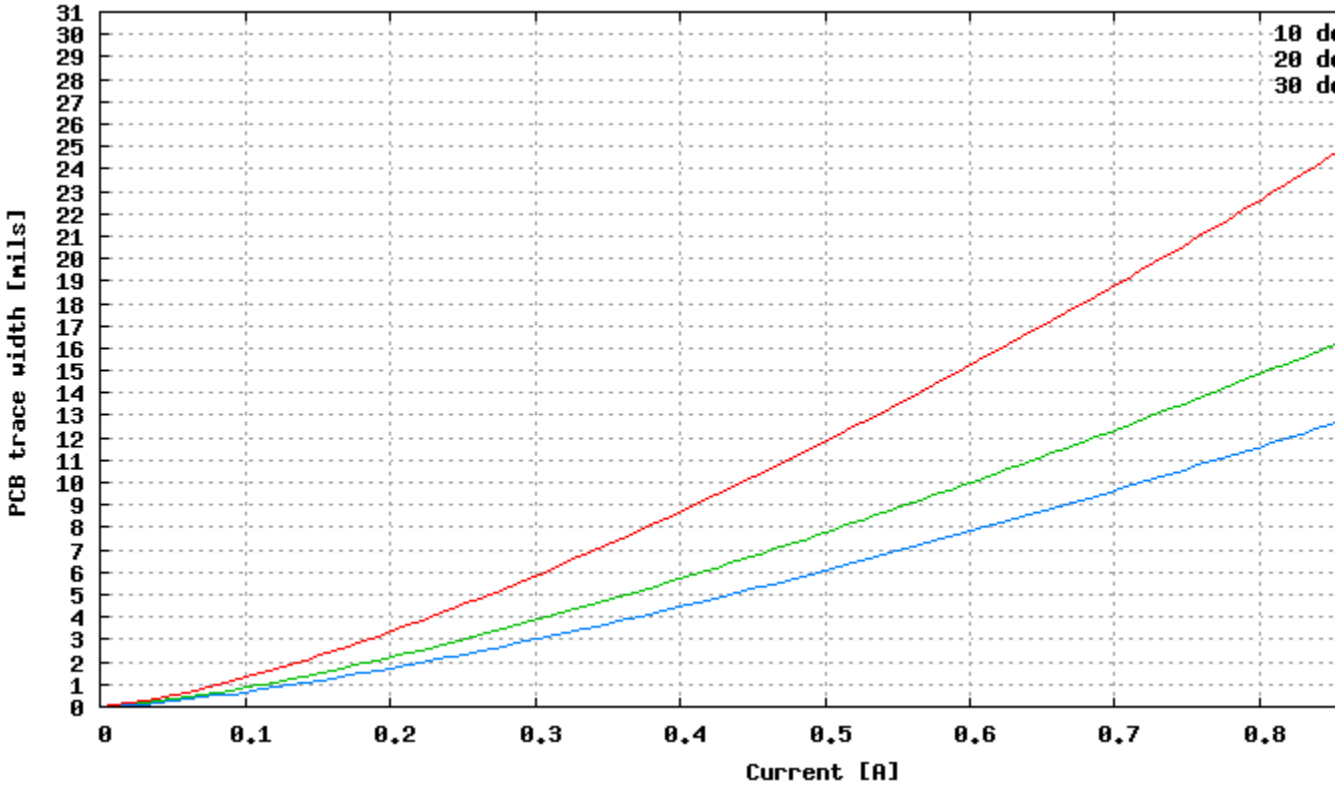
Outer traces (0-1 A)



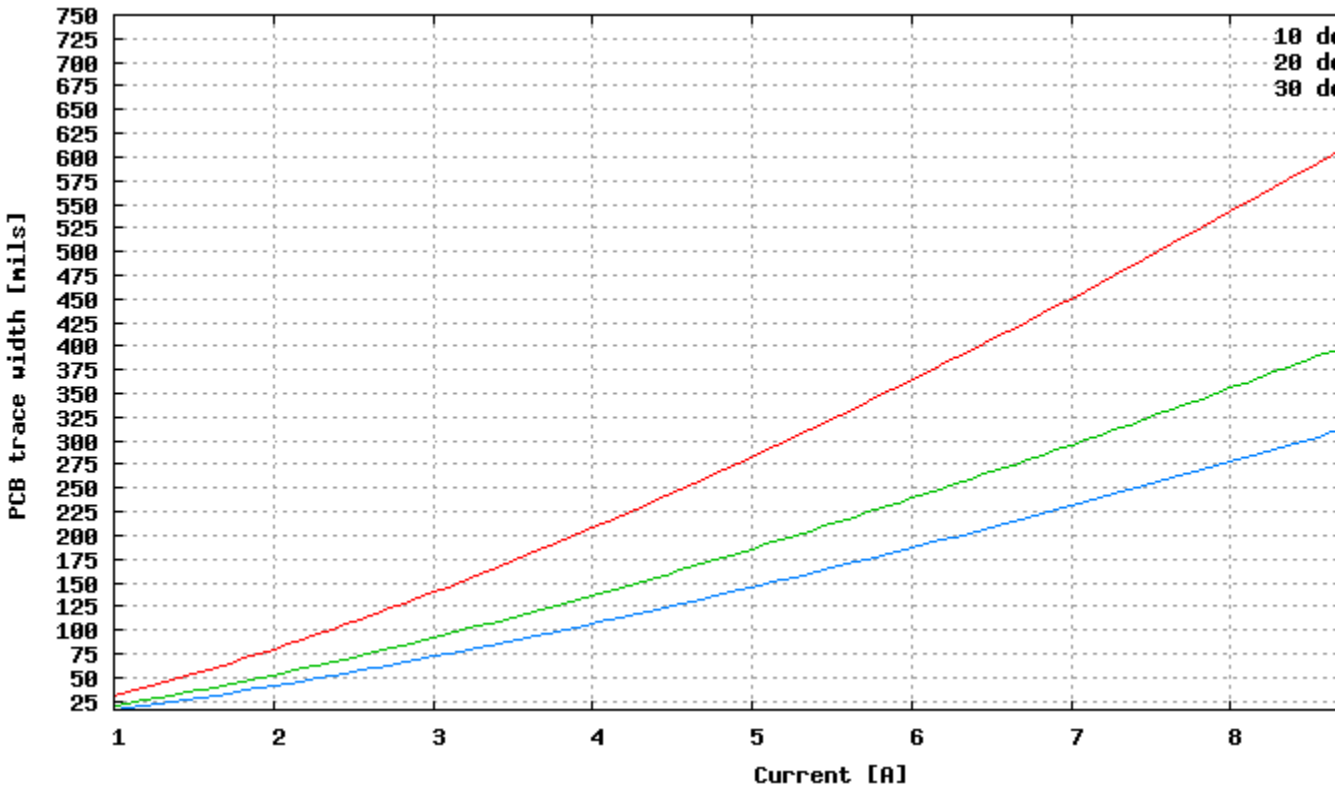
Outer traces (1-10 A)



Inner traces (0-1 A)



Inner traces (1-10 A)



Formula

Given:

- I [A] *(Current)*
- T [°C] *(Temperature rise)*
- m [oz] *(Mass of PCB trace)*

Constants:

- y = 1.378 *[mils/oz] for copper*
- b = 0.44
- c = 0.725
- k = 0.048 *(for outer layers)*
- k = 0.024 *(for inner layers)*

Formulas:

- A [mils²] = $\left(\frac{I}{kT^b}\right)^{\frac{1}{c}}$ *(PCB trace area)*
- l [mils] = $\frac{A}{my}$ *(PCB trace width)*

Links

- UltraCAD article: Current Carrying Capacity of Vias (http://www.ultracad.com/articles/viacurrents.pdf)
- PCB Trace Width Calculator (http://circuitcalculator.com/wordpress/2006/01/31/pcb-trace-width-calculator/) by Brad Suppanz
- New Correlations Between Electrical Current and Temperature Rise in PCB Traces (http://www.flomerics.com/flotherm/technical_papers/t341.pdf) by Johannes Adam at Flomerics Ltd.

Retrieved from "http://www.hardwarebook.info/PCB_trace"

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