The opinion in support of the decision being entered today was *not* written for publication and is *not* binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte, MARK D. FRANK, JERIMY NELSON, and NATHAN BERTRAND

Appeal 2006-3123
Application 10/368,789
Technology Center 2800

Decided: February 16, 2007

Before JAMES D. THOMAS, MAHSHID D. SAADAT, and ALLEN R. MACDONALD, *Administrative Patent Judges*.

MACDONALD, *Administrative Patent Judge*.

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134 from the Examiner's rejection of claims 1-6, 8-10, 16, 17, and 19-21. We note that the Examiner has indicated that claims 11-14 and 18 stand objected to and would be allowable if rewritten in independent form including all the

limitations of the base claim and any intervening claims (Answer 5). Claims 7 and 15 have been cancelled.

THE INVENTION

The disclosed invention pertains to a system and method for evaluating power and ground vias in a package design. In one aspect, a method evaluates vias in an electronic design. The method includes the step of formulating one or more via sufficiency rules, and then processing the electronic design to determine whether the vias of the electronic design violate the via sufficiency rules. In the event of a violation, the method further includes generating an indicator associated with the electronic design to identify vias that violate the via sufficiency rules. The step of generating an indicator can include generating a visual indicator (e.g., a via insufficiency Design Rule Check (DRC)) on a graphical user interface depicting the electronic design, and/or a textual report summarizing the violations. In another aspect, the step of processing includes the step of processing one or more selected layers of the electronic design for violation of the via sufficiency rules (Specification 5).

Representative claim 1 is illustrative:

1. A method for evaluating power and ground vias in an electronic design, comprising the steps of:

formulating one or more via sufficiency rules;

processing the electronic design to determine whether the power and ground vias of the electronic design violate the via sufficiency rules; and

generating an indicator associated with the electronic design to identify vias that violate the via sufficiency rules.

THE REFERENCE

The Examiner relies upon the following reference as evidence of anticipation:

Yu	US 6,829,754 B1	Dec. 7, 2004 (filed Jun. 4, 2002)

THE REJECTION

The following rejection is on appeal before us:

1. Claims 1-6, 8-10, 16, 17, and 19-21 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Yu.

Rather than repeat the arguments of Appellants or the Examiner, we make reference to the Briefs and the Answer for the respective details thereof.

OPINION

We have carefully considered the subject matter on appeal, the rejection advanced by the Examiner and the evidence of anticipation relied upon by the Examiner as support for the rejection. We have, likewise, reviewed and taken into consideration, in reaching our decision, the Appellants' arguments set forth in the Briefs along with the Examiner's rationale in support of the rejection and arguments in rebuttal set forth in the Examiner's Answer.

It is our view, after consideration of the record before us, that the evidence relied upon supports the Examiner's rejection of claims 1, 2, 16, 17, 20, and 21, but does not support the Examiner's rejection of claims 3-6, 8-10, and 19. Accordingly, we affirm-in-part.

GROUPING OF CLAIMS

We consider separately the anticipation of each claim on appeal, as designated under separate subheadings and argued separately by Appellants in the Briefs.

Claim 1

Appellants argue that Yu does not disclose *formulating* one or more via sufficiency rules as required by step (a) of claim 1 (emphasis added). Appellants contend that Yu merely discloses a via analysis specific to an ASIC power design (emphasis added). Appellants further assert that Yu fails to disclose via checking for layers of a *package design*, and therefore cannot anticipate claim 1 (Br. 10).

The Examiner disagrees. The Examiner finds that Yu's via checker 214 checks for a minimum number of vias by applying special via rules (*See* Yu, col. 11, ll. 51-67). The Examiner notes that power checker program 100 and via checker 214 generate an error indicator when an insufficient via array is detected (*See* Yu col. 11, ll. 46-67). The Examiner notes that Fig. 10 explicitly discloses errors based on via rules (*See* Yu, Fig. 10, Rules 6.1, 6.2, 6.3, 6.4, and 6.5; *see also* col. 8, ll. 9-11, ll. 34-35; col. 9, ll. 44-46; col. 11, ll. 19-23, ll. 46-67, col. 12, ll. 1-34). The Examiner finds that Yu's power checker program 100 determines whether power and ground vias of the electronic design violate via sufficiency rules. Thus, the Examiner concludes that Yu fully discloses the recited limitations. The Examiner contends that Appellants are arguing limitations described in the Specification that are not claimed (Answer 5).

After carefully reviewing all the evidence before us, we will sustain the Examiner's rejection of claim 1 for essentially the same reasons argued by the Examiner in the Answer. In particular, we agree with the Examiner that Appellants are arguing limitations from the Specification. Patentability is based upon the claims. "It is the claims that measure the invention." *SRI Int'l v. Matsushita Elec. Corp.of America*, 775 F.2d 1107, 1121, 227 USPQ 577, 585 (Fed. Cir. 1985) (*en banc*). A basic canon of claim construction is that one may not read a limitation into a claim from the written description. *Renishaw plc v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1248, 48 USPQ2d 1117, 1120 (Fed. Cir. 1998). Although the claims are interpreted in light of the specification, limitations from the specification are not read

into the claims. *In re Van Geuns*, 988 F.2d 1181, 1184, 26 USPQ2d 1057, 1059 (Fed. Cir. 1993).

In the instant case, we find no basis for Appellants' contention that Yu cannot anticipate claim 1 because Yu does not disclose via checking for layers of a *package design* (*see* Br. 11). In particular, we note that the step of checking for layers of a *package design* is not recited in claim 1. With respect to Appellants' argument that Yu fails to disclose *formulating* one or more via sufficiency rules, we note that Yu explicitly discloses via Rules 6.1, 6.2, 6.3, 6.4, and 6.5 that generate an error, e.g., (1) if the number of vias is *less than the minimum* recommended, or (2), if the vias are *insufficient* at a strap connection, or (3), if the vias are *missing* or *not fully populated* (*See* Fig. 10). We find that Yu's via sufficiency Rules 6.1, 6.2, 6.3, 6.4 and 6.5 are inherently formulated. Thus, we agree with the Examiner that Yu fully discloses the recited limitations of independent claim 1.

Claim 2

Appellants note that claim 2 recites the step of "processing one or more selected layers of the electronic design for violation of the via sufficiency rules" (Br. 11). Appellants argue that Yu does not disclose or suggest processing selected layers of the electronic design (*id.*). In particular, Appellants argue that Yu does not disclose the *selecting of layers* (*id.*, emphasis added).

The Examiner disagrees. The Examiner notes that a via is a connection between at least two or more layers. The Examiner asserts that Yu's power checker program processes *one or more selected layers* of the

ASIC design for violations of the via sufficiency rules (col. 11, ll. 19-23) (emphasis added). Thus, the Examiner concludes that Yu discloses the recited limitations (Answer 7).

We will sustain the Examiner's rejection of claim 2 for essentially the same reasons argued by the Examiner in the Answer. We agree with the Examiner that Yu's power checker program processes *one or more selected layers* of the ASIC design for violations of via sufficiency rules. In particular, we note that Yu broadly discloses substrate 66 and die 62 as layers of an electronic design (Fig. 2, col. 3, l. 22). Thus, we find that the layers of Yu's electronic design are processed as necessary to detect violations of via sufficiency rules (*see* "Via Checker" discussion, col. 11, ll. 46-67).

Claim 3

Appellants argue that Yu fails to disclose a via sufficiency rule defining a via per pad count for one layer of the electronic design (Br. 11).

The Examiner disagrees. The Examiner notes that Rule 6.1 generates an error if the number of vias is less than the minimum recommended for a standard cell rail (Fig. 10). The Examiner points out that these power and/or ground metal lines (i.e., "rails") are intersected by vias to provide power to a standard cell. The Examiner further notes that Yu's "via checker" program flags an error when the number of via at the intersection is insufficient, as determined by Yu's via sufficiency rules (col. 5, ll. 60-63). The Examiner concludes that Yu's via checker program must count the number of vias at intersections in *each layer* in order to check for the proper number of vias (Answer 11).

We will reverse the Examiner's rejection of claim 3 because we agree with Appellants that Yu fails to disclose a *via sufficiency rule* that explicitly or inherently defines a *via per pad count* for *one layer* of the electronic design. While we agree with the Examiner that Yu *suggests* the limitations of the claim, we note that our reviewing court has determined that anticipation requires every element and limitation of the claimed invention to be found in a single prior art reference, arranged as in the claim. *Karsten Mfg. Corp. v. Cleveland Golf Co.,* 242 F.3d 1376, 1383, 58 USPQ2d 1286, 1291 (Fed. Cir. 2001); *Scripps Clinic & Research Foundation v. Genentech, Inc.,* 927 F.2d 1565, 1576, 18 USPQ2d 1001, 1010 (Fed. Cir. 1991). In the instant case, we find that Yu's Rules 6.1, 6.2, 6.3, 6.4, and 6.5 are silent with respect to a specific *via per pad count* for *one layer* of the electronic design.

Claims 4-6, and 8-10

Because dependent claims 4-6 and 8-10 each include the limitations of claim 3, we will also reverse the Examiner's rejection of these claims for the same reasons discussed *supra* with respect to claim 3.

Claim 16

Appellants argue that Yu fails to disclose determining instances of power and ground via sufficiency in a package design, as claimed. In particular, Appellants argue that Yu does not disclose via sufficiency rules for a package design (Br. 13).

The Examiner disagrees (Answer 5). See the Examiner's response for claim 1, *supra.*

We will sustain the Examiner's rejection of independent claim 16 for essentially the same reasons argued by the Examiner in the Answer and discussed *supra* with respect to independent claim 1. In addition, we find that Yu discloses determining instances of power and ground via sufficiency in a package design. *See* col. 11, ll. 60-62, i.e., "The minimum number of vias to be used in the special via rule for producing vias for standard cell power/ground routing to the mesh is determined by a library," *see also* col. 11, ll. 19-24, and col. 5, ll. 62-65. We also find that Yu discloses via sufficiency rules for a package design, as discussed *supra* (*see* Fig. 10, Rules 6.1, 6.2, 6.3, 6.4 and 6.5).

Claim 17

Appellants argue that Yu fails to disclose formulating one or more via sufficiency rules (Br. 13).

The Examiner disagrees (Answer 5). See the Examiner's response for claim 1, *supra*.

We have noted *supra* that Yu explicitly discloses via sufficiency rules 6.1, 6.2, 6.3, 6.4 and 6.5 (*See* Fig. 10). We find that Yu's via sufficiency rules are inherently formulated, as discussed *supra* with respect to claim 1.

Claim 19

Appellants point out that claim 19 recites one of the via sufficiency rules defines a power and ground *via count per pad for one layer* of the electronic design, and includes determining whether each layer of the electronic design has a requisite number of power and ground vias associated with each pad of the one layer.

We agree with Appellants that Yu fails to disclose a *via sufficiency rule* that explicitly or inherently defines a *via count per pad for one layer* of the electronic design. Therefore, we will reverse the Examiner's rejection of dependent claim 19 for the same reasons discussed *supra* with respect to dependent claim 3.

Claim 20

Appellants argue that Yu fails to disclose or suggest responding to designer input to scope the instructions for determining instances of power and ground vias (Br. 14).

The Examiner disagrees (Answer 11). The Examiner notes that Yu discloses a via checker that verifies a minimum number of vias to be used in the special via rule for producing vias for a standard cell power/ground routing to the mesh within the ASIC design (col. 11, ll. 53-65). The Examiner notes that Yu discloses if the user moves the cursor over an error marker, a text description of the error will pop up (e.g., indicating insufficient via array size, VDD/VSS, short unconnected VDD/VSS) (col. 5, ll. 62-65) (Answer 11). The Examiner asserts that the process of moving the cursor by the user or designer corresponds to "responding to designer inputs to scope the instructions for determining instances of power and ground vias," as claimed (*id.*).

We note that Yu discloses responding to designer input to scope the instructions for determining instances of power *elements*:

> The method further includes providing a user with a choice of which power elements in the design to check, and executing the power checker modules

> corresponding to the selected power elements in order to check for errors in the selected power elements. Any detected errors are output for the user.

(col. 2, ll. 24-29 and col. 11, ll. 19-24)

We further note that Yu discloses power and *ground* elements at column 11, lines 19-24, and line 65 (i.e., VDD and VSS, respectively). Because Yu also discloses that vias are used to deliver power to the various layers, we find that Yu discloses all that is claimed (*See* e.g., col. 11, ll. 19-24, and ll. 48-50). Therefore, we will sustain the Examiner's rejection of claim 20 as being anticipated by Yu.

Claim 21

Appellants argue that Yu fails to disclose formulating one or more via sufficiency rules, or processing the electronic design to determine whether the power and ground vias of the electronic design violate one or more of the via sufficiency rules (Br. 14).

The Examiner disagrees (Answer 5). See the Examiner's response for claim 1, as discussed *supra*.

We note that we have found *supra* that Yu discloses formulating one or more via sufficiency rules, and processing the electronic design to determine whether the power and ground vias of the electronic design violate one or more of the via sufficiency rules. See discussion of claims 1 and 16, *supra*. Therefore, we will sustain the Examiner's rejection of

independent claim 21 as being anticipated by Yu for the same reasons argued by the Examiner and discussed *supra*.

DECISION

We sustain the Examiner's rejection of claims 1, 2, 16, 17, 20, and 21, but we reverse the Examiner's rejection of claims 3-6, 8-10, and 19. Therefore, the decision of the Examiner rejecting claims 1-6, 8-10, 16, 17, and 19-21 is affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART.

kis /GW

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