

The opinion in support of the decision being entered
today is *not* binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte HARRY LIU, LONNY BERG, WILLIAM L. LARSON, SHAOPING LI,
THEODORE ZHU, and JOEL DREWES

Appeal 2006-3363
Application 10/873,363
Technology Center 2800

Decided: September 26, 2007

Before JAMES D. THOMAS, JOSEPH F. RUGGIERO, and ROBERT E. NAPPI,
Administrative Patent Judges.

NAPPI, *Administrative Patent Judge*.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 of the final rejection of claims 1 through 6. For the reasons stated *infra*, we affirm the Examiner's rejection of these claims.

INVENTION

The invention is directed to a method of making magneto-resistive bits where the bits are protected against later process steps that could damage unprotected bits. The method provides protection by encapsulating the bit with a etch stop barrier to cover the top and side walls of the bit. See page 3 of Appellants' Specification. Claim 1 is representative of the invention and reproduced below:

1. A passivated magneto-resistive bit structure, comprising:
 - a magneto-resistive bit having a top surface and side walls;
 - a conductive etch stop barrier layer encapsulating the top surface and side walls of said bit; and
 - a metal contact provided upon at least part of said etch stop barrier layer.

REFERENCE

The reference relied upon by the Examiner is:

Tehrani US 5,861,328 Jan. 19, 1999

REJECTION AT ISSUE

Claims 1 through 6 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Tehrani. The Examiner's rejection is set forth on page 4 of the Answer.

Throughout the opinion, we make reference to the Brief and Reply Brief (filed March 3, 2006 and June 6, 2006 respectively), and the Answer (mailed April 6, 2006) for the respective details thereof.

OPINION

Appellants argue that Tehrani does not teach a magneto-resistive bit encapsulated by a conductive etch stop layer as claimed. Appellants state that Tehrani teaches two distinct embodiments, one in which vias 47 and 50 are etched separately and the other where vias 47 and 50 are etched in the same operation. Appellants argue that the Examiner's rejection is mixing embodiments, asserting that in the first embodiment the magneto-resistive bit is encapsulated by a dielectric layer, but that in the second embodiment, which uses a conductive etch stop layer, Appellants argue the etch stop layer is not on the sides of the magneto-resistive bit. Brief p. 3. Appellants state that in the second embodiment Tehrani identifies that the etching of the vias 50 must not extend outside the magneto-resistive bit. Appellants reason that this is because the conductive bit stop layer is not present to provide protection on the sides of the magneto-resistive bit. Brief pp. 4-5. Appellants also reason that the conductive bit stop layer of the second embodiment does not cover the same area as the dielectric layer of the first embodiment since, if this were the case, the conductive bit stop layer would short out the circuit. Brief p. 5.

The Examiner responds, on page 7 of the Answer, stating that in the second embodiment, where the vias are etched simultaneously, the same chemistry is used to form both vias. The Examiner cites to column 5, lines 58-62 of Tehrani as describing that to protect the magneto resistive element (bit) from corrosive agents, the vias 50 must be enclosed and may not extend outside the ends of the bit.

Answer p. 7. The Examiner states "Tehrani does not indicate that it [the via being enclosed by and not extending outside the ends of the bit] is because there is no conductive barrier on the sidewalls of the bit." Answer p. 9. Further, the Examiner finds that the cap layer 45 "completely seals the bit structure 41 and

provides a barrier to moisture, oxidation, and corrosive agents (see, e.g., col. 5/ll. 1-4 and fig. 5).” Answer p. 7. The Examiner finds that “[t]he difference between the cap layers of the first and second processes is that in the first process the first layer of the dielectric cap 45 is an insulating barrier and in the second process it is a conductive etch stop barrier layer (see, e.g., col. 5/ll.55-58 and col.5/ll.67-col.6/ll.2).” Answer pp. 7-8. Further, the Examiner does not find that Tehrani teaches that the first layer extends everywhere the dielectric cap is shown. Answer p. 8. The Examiner summarizes:

Appellants' conclusion that the etch stop barrier layer is not on the sidewalls of the bit is not described by Tehrani. What is clearly described by Tehrani is the fact that the first layer of the cap layer 45 completely seals the bit 41 (see, e.g., col.5/ll.4-8), and that in the second process, this first layer is CrSi, which is the same conductive etch stop barrier material of the claimed invention (see, e.g., col. 5/ll.55-58 and col.5/ll.67-col.6/ll.2).

Answer p. 10.

Thus, the issue before us is whether there is substantial evidence to support the Examiner's finding that Tehrani teaches “a magneto-resistive bit having a top surface and side walls; a conductive etch stop barrier layer encapsulating the top surface and side walls of said bit” as recited in claim 1.

FINDINGS OF FACT

1. Tehrani teaches a method of fabricating giant magneto-resistive (GMR) devices on a substrate with a semiconductor device formed thereon. The method includes forming a cap on the GMR cell to seal the cell and provide a barrier to subsequent operations.

Abstract.

2. After the underlying semiconductor device is fabricated, a dielectric system, item 32, is formed over the semiconductor device. Col. 3, ll. 60-62.
3. This dielectric system 32 provides a smooth surface to deposit the GMR material and has properties to provide a barrier for moisture and oxidation. Col. 4, ll. 5-11, 20-24.
4. A layer of GMR material is formed on top of dielectric system 32 and formed into a magnetic memory cell. Col. 4, ll. 36- 44.
5. A dielectric cap is formed over the magnetic memory cell. Col. 4, l. 67 – col. 5, l. 4.
6. Tehrani states “[c]ap 45 is provided to seal GMR memory element 41 and provide a barrier to moisture, oxidation, and corrosive agents for subsequent operations and permanent use. Dielectric cap 45 includes at least one barrier layer which, in conjunction with the barrier properties of dielectric system 32 beneath GMR memory elements 41, seals elements 41 in a substantially complete barrier.” Col. 5, ll. 1-8.
7. From this disclosure, we find that one skilled in the art would recognize that one layer of cap 45 covers and provides protection of the top and sides of the GMR element while the dielectric system 32 provides protection of the bottom of the GMR element.
8. The dielectric cap consists of several layers of different materials, one of which masks the barrier layer for etching. Col. 5, ll. 8-21.
9. Tehrani teaches that there are two methods of etching the vias 47 (which are through both layers 45 and 32) and vias 50 (which are through parts of layer 45). See figure 7.

10. In the first method, vias 47 and 50 are etched in different processes. Vias 47 are etched through both the dielectric cap 45 and 32 in one step using convention etching methods such as reactive ion etch (RIE). Note, the GMR element is protected in this step by cap and dielectric system discussed in fact 7. The vias 50 are then etched through dielectric cap 45 using two etching steps, the first to an etch stop layer using conventional etching methods. After the etch stop layer is removed from via 50, the via is etched again to the depth of GMR element. This second etching of via 50 is performed using different chemistry which does not damage the GMR element. Col. 5, ll. 22-53.
11. In the via forming method of fact 10, the via areas 50, may be outside the end of the GMR layer. Col. 5, ll. 36-38
12. In the second method of etching vias 47 and 50, both vias are formed in a single operation. Col. 5, ll. 54-55.
13. In the second method of etching vias 47 and 50, the first layer of dielectric system 45 is conductive etch stop material. Col. 5, ll. 55-56, col. 6, ll. 9-11.
14. In the second method, the etch stop layer is made of a material that is unreactve to RIE etches (which are corrosive to GMR material). Thus, via 50, is etched to the depth of the etch stop. Col. 5, ll. 65-67.
15. In the second method, the vias 50 must not extend beyond the ends of the GMR element. This is to protect the GMR element from the stripping process. Col. 5, ll. 59-62.

PRINCIPLES OF LAW

“Substantial evidence ‘means such relevant evidence as a reasonable mind might accept as adequate to support a conclusion.’” *In re Jolley* 308 F.3d 1317, 1320, 64 USPQ2d 1901, 1903 (Fed. Cir. (2002)) (citing *Consol. Edison Co. v NLRB*, 305 U.S. 197, 229 (1938)). “[T]he possibility of drawing two inconsistent conclusions from the evidence” will not render a decision unsupported by substantial evidence. *Id.*, (citing *Consolo. v. Fed. Mar. Comm'n*, 383 U.S. 607, 620 (1966)).

ANALYSIS

Appellants’ arguments have not persuaded us of error in the Examiner’s rejection. Initially, we note that the Appellants’ arguments on pages 4 through 6 of the Brief and 2 through 4 of the Reply Brief are directed to the drawings of Tehrani being inconclusive of the facts found by the Examiner. We note that the standard of review is whether there is substantial evidence of record (evidence that a reasonable mind will accept as adequate). This standard will permit a finding to be supported by the evidence even if inconsistent conclusions can be drawn from the evidence. See *In re Jolley, supra*.

Tehrani teaches that the first layer of dielectric cap 45 provides a barrier which seals the GMR element. This layer in conjunction with layer 32 below seals the GMR element, thus the layer of cap 45 covers the sides of GMR element. Facts 6 and 7. In the embodiment where the vias 47 and 50 are etched separately, vias 50 can extend beyond the edges of the GMR as the etching with the process that can damage GMR stops above the barrier layer. Fact 10. We note, that stopping at this level means that the etching is stopped above the GMR element and above dielectric system 32. In the embodiment where the vias 47 and 50 are etched simultaneously, the etching stops at the etch stop layer which is formed on

the GMR element. Facts 13 and 14. In this embodiment, the etching must be within the edges to prevent the GMR element from being damaged by the etching step. Fact 15.

From these facts, we do not find that evidence contradicts the Examiner's finding that the conductive etch stop layer, of layer 45, covers and provides protection of the top and sides of the GMR element. Tehrani does not explicitly state that this also applies to the embodiment where vias 47 and 50 are etched simultaneously and a conductive etch stop is used. As Appellants assert, keeping the vias 50 within the edge of the GMR element could suggest that the conductive etch stop is not on the side of the GMR element. However, we note, in this embodiment, for the etching step to create vias 47, the etching step must be able to etch both layers 45 and dielectric system 32. As discussed above, the layer 32 also provides protection to the GMR element. One skilled in the art would recognize that the teaching of keeping vias 50 within the edges of the GMR element, also prevents the etching step from etching the dielectric system 32 which is protecting the underside of GMR element (i.e. even with the etch stop on the side of the GMR material, if the etching process compromised dielectric system 32 the GMR would be exposed from below). Thus, we find evidence of record to support the Examiner's conclusion which is contrary to that asserted by Appellants. As the substantial evidence standard does not preclude a finding when inconsistent conclusions can be drawn from the evidence, we find that there is substantial evidence to support the Examiner's findings.

Appellants also argue that the conductive bit stop layer of the second embodiment does not cover the same area as the dielectric layer of the first embodiment because, if so, it would short out the circuit. Thus, Appellants assert that the embodiment which uses a conductive bit stop for the first layer differs

from the embodiment which uses a dielectric for the first layer. Accordingly, Appellants conclude that the conductive bit stop is not on the sides of the GMR element. Brief p. 5. Appellants' argument is not persuasive since we find that the conductive bit stop layer is patterned. This patterning is necessary since, if not done, the etch stop layer would prevent vias 47 from being etched through both layers 45 and 32. However, we do not find that, because the conductive bit stop layer is patterned, one of skill in the art would conclude that the conductive bit stop layer is not on the sides of the GMR element.

For the forgoing reasons, the Appellants have not convinced us that the Examiner's finding that Tehrani teaches "a magneto-resistive bit having a top surface and side walls; a conductive etch stop barrier layer encapsulating the top surface and side walls of said bit" is unsupported by substantial evidence. Accordingly, we find no error in the Examiner's rejection of claims 1 through 6.

CONCLUSION

The decision of the Examiner is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv) (2006).

AFFIRMED

tdl/ce

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