

The opinion in support of the decision being entered today was *not* written for publication and is *not* binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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*Ex parte Donald Joe Deaton*

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Appeal 2006-3382  
Application 10/461,709<sup>1</sup>  
Technology Center 2800

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Decided: March 29, 2007

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*Before KENNETH W. HAIRSTON, HOWARD B. BLANKENSHIP, and  
JAY P. LUCAS, Administrative Patent Judges.*

LUCAS, *Administrative Patent Judge.*

DECISION ON APPEAL

STATEMENT OF CASE

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<sup>1</sup> Application filed June 13, 2003. Appellant claims the benefit under 35 U.S.C. § 119 of provisional application 60/388,539, filed 06/13/2002. Application 11/174,368 is a continuation of 10/461,709, and has issued as Patent No. 7,009,370 on 03/07/2006. The real party in interest is DRS Test & Energy Management, Inc. of Huntsville, Alabama.

Appellant appeals from a final rejection of claims 1, 2, 4, 5, 7, 8, 14-22, 28-51, 53-55, and 57-62 under authority of 35 U.S.C. § 134 (2002). The BPAI has jurisdiction under 35 U.S.C. § 6(b)(2002).

Appellant's invention relates to a circuit for delivering high power current pulses to an electronic load in an efficient manner. In the words of the Appellant:

The present invention comprises a scalable, interleaved pulse forming converter having 2 Buck switching converter modules each contributing half to the total load of the circuit. Synchronization pulses to the two modules are set 180 degrees out of phase of each other to reduce ripple current. Additional embodiments are also claimed in which module interleaving may be utilized to further reduce ripple current and increase power, as well as to electrically isolate the load from input or battery ground.

Claim 1 and Claim 57 are exemplary and representative:

1. A circuit for providing an electrical pulse to a load, comprising:
  - a. a first Buck converter circuit;
  - b. a second Buck converter circuit connected to said first Buck converter circuit, each said Buck converter circuit adapted to receive a current command signal for establishing an internal reference voltage within each said Buck converter circuit;
  - c. means for applying a voltage across said first and said second Buck converter circuits;
  - d. a capacitor connected in parallel with said voltage means for reducing ripple in said voltage across said first and said second Buck converter circuits;
  - e. a synchronization controller operationally connected to each said Buck converter circuit for initiating electrical pulses in

each said Buck converter circuit in interleaved fashion to produce a controllable pulse across said load; and,

- f. wherein said first and second Buck converters are arranged such that a unidirectional current pulse is generated across said load.

57. A circuit for providing an electrical pulse to a load, comprising:

- a. a first Buck converter circuit;
- b. a second Buck converter circuit connected to said first Buck converter circuit, each said Buck converter circuit adapted to receive a user selectable current command signal for controlling the magnitude of said electrical pulse generated across said load;
- c. means for applying a voltage across said first and said second Buck converter circuits;
- d. a capacitor connected in parallel with said voltage means for reducing ripple in said voltage across said first and said second Buck converter circuits;
- e. a synchronization controller operationally connected to each said Buck converter circuit for initiating electrical pulses in each said Buck converter circuit in interleaved fashion to produce a controllable pulse across said load; and,
- f. wherein each said Buck converter is electrically arranged in serial with said load.

Group I: The Examiner rejected claims 1-2, 4-5, 7, 14, 17-18, 20-21, 28-30, 32-34, 37-38, 40-42, 46-51, 53-55, and 57-62 under 35 U.S.C. § 102(b) (2004) for being anticipated by Golaszek.

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Group II: The Examiner rejected claims 8, 15-16, 19, 22, 31, 36, and 39 under 35 U.S.C. § 103(a) for being obvious over Goluszek in view of Wang.

Group III: The Examiner rejected claims 35, and 43-45 under 35 U.S.C. § 103(a) for being obvious over Goluszek.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Goluszek	US 6,211,657	Apr. 3, 2001
Wang	US 6,518,738	Feb. 11, 2003

Appellant contends that the claimed subject matter is not anticipated by Goluszek, or rendered obvious by Goluszek alone, or in combination with Wang, for reasons to be discussed more fully below. The Examiner contends that each of the three groups of claims is properly rejected.

Rather than repeat the arguments of Appellant or the Examiner, we make reference to the Briefs and the Answer for their respective details. Only those arguments actually made by Appellant have been considered in this decision. Arguments which Appellant could have made but chose not to make in the Briefs have not been considered and are deemed to be waived.

*See 37 C.F.R. § 41.37(c)(1)(vii)(2004).<sup>2</sup>*

We affirm the rejections.

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<sup>2</sup> Appellant has not presented any substantive arguments directed separately to the patentability of the dependent claims or related claims in each group, except as will be noted in this opinion. In the absence of a separate argument with respect to those claims, they stand or fall with the representative independent claim. *See In re Young*, 927 F.2d 588, 590, 18 USPQ2d 1089, 1091 (Fed. Cir. 1991). *See also* 37 C.F.R. § 41.37(c)(1)(vii).

## ISSUE

The issue is whether Appellant has shown that the Examiner erred in rejecting the claims under 35 U.S.C. § 102(b) and 103(a). The issue turns on a number of specific issues relevant to the limitations of the specific claims.

## FINDINGS OF FACT

Concerning the rejection of claims 1-2, 4-5, 7, 14, 17-18, 20-21, 28-30, 32-34, 37-38, 40-42, 46-51, 53-55, 57-62 under 35 U.S.C. § 102(b)(2004) for being anticipated by Goluszek.

1. Appellant has invented a circuit for an improved pulse forming interleaved current converter. (Specification 1).
2. Examiner has rejected (final) the claims noted above for being anticipated by Goluszek, which teaches a power converter using interleaved Buck regulators. (Answer 3).
3. Referring to Figures 3 and 5 of Goluszek, Examiner has read the claimed first Buck converter circuit on elements switch 60, diode 81 and inductor 65; the second Buck converter circuit on corresponding elements 70, 78 and 75; a command signal coming from operational amplifier 108 for establishing an internal reference voltage; means 56 for applying a voltage across the two Buck converters; a capacitor in parallel with the voltage means on capacitor 76; a synchronization controller connected to the Buck converters to initiate pulses in interleaved fashion is read on controllers 102 and 110; and the unidirectional current pulse as Goluszek's regulated DC pulse train.

Goluszek demonstrates the claimed common ground of claims 2 and 33 as the negative pole of the power source 56, and transistor switches 60 and 70. Details of the rejection of the other claims in this group are presented in the Answer.

4. Appellant contends that the presence of capacitor 77 (e.g. in Goluszek's Figure 3) renders the teaching of Goluszek non-anticipatory (Br. 9). Appellant contends that capacitor 77 smoothes the DC pulse stream of Goluszek so it no longer meets the claim limitation, indeed Appellant contends Goluszek teaches away from the claimed subject matter. Considering Figures 3 and 5 of the reference, we find that Goluszek states that smoothing of the pulses is merely further processing of the DC pulses produced by the interleaved Buck regulators. This does not obviate the teaching, but merely demonstrates that Goluszek uses the claimed power regulators as only part of his full invention. "Teaching away" requires a negation of the teaching (see below); Goluszek merely goes on to further process the DC pulses in accordance with his own invention.
5. Appellant contends, in the footnote of his Brief (page 10), that Goluszek's drafter erred in calling the output of his first stage DC pulses or modulated DC pulses. We find, rather, that the output of the first stage was accurately portrayed, but that the input to his second stage was preprocessed by the capacitor. The teaching of Goluszek of pulses is sound, and further processing of the signals to effect another invention does not obviate it.

6. Appellant further argues that claims 5, 7, 14, 18, 21, 30, 34, 38, and 41 claim sensing of the current levels of the transistor switches in the two Buck circuits, which he alleges is not shown in Goluszek. Examiner contends that the “error amplifiers measure the inductor currents [which are] the same currents that flow through the transistors 60, 70. Therefore the output current of [the] transistors are also measured.” Referring to Goluszek’s Figure 5, we note that the current flowing through transistor switch 60 also flows through inductor 65 (diode 81 being non-conducting to that current). Thus we find the Examiner’s contention accurate.
7. With regard to claims 32 and 40, the limitation “adapted to receive a current command signal” is noted. We find, however, that the output of Goluszek’s amplifiers 104 and 112, called current error amplifiers in that reference, creates a set of signals that are the command signals as claimed.
8. With respect to claims 57-60, we are drawn to carefully consider the scope and meaning of the phrase “adapted to receive a user selectable current command signal for controlling the magnitude of said electrical pulse generated across said load.” Appellant contends that the term must be viewed in terms of the Specification, which recites that the user’s selection may be from such means as “adjusting a potentiometer, or from a D-to-A (‘digital-to-analog’) converter that receives the amplitude setting from a computer.” (Specification 8). In Goluszek, Appellant contends, one merely has a set error signal

feeding back from the output, and “the error signal of amplifier 108 is not selectively set by a user because only the gain of the amplifier may be set by the user.” (Reply Br. 8). The Examiner contends that the “user” does set the selectable current command signal, since the user specifies the relative size of the voltage splitting resistors on the output (Goluszek, Fig. 5), which drives the firing of current error amplifiers 104 and 112, and the controllers 102, 110. In giving claims their broadest reasonable interpretation, and in avoiding reading limitations from the Specification that do not appear in the claims, we find that the claims do read on the Goluszek reference when viewed as expressed by the Examiner. The claims do not require that the command signal can be easily modified during use, as by a potentiometer, but only that they can be user selected.

Concerning the rejection of claims 8, 15-16, 19, 22, 31, 36, and 39 under 35 U.S.C. 103(a) for being obvious over Goluszek in view of Wang.

1. Examiner contends that Goluszek does not show the details of the Pulse Width Modulator as being comprised of a set-reset RS flip flop. Wang does show that the PWM can be so comprised, in the context of a switching regulator control circuit. (Answer 8). Appellant does not argue against that specific contention, but relies instead on the general issues raised above concerning Goluszek’s design and the pulses entering the second stage. (Br. 13). We find that the Examiner’s combination of references does render the noted claims obvious over the art.

Concerning the rejection of claims 35, and 43-45 under 35 U.S.C. § 103(a) for being obvious over Goluszek.

1. Examiner contends that Goluszek teaches all of the claimed limitations except for the laser diode load, as specified in these. He contends that such a load would be an obvious substitution of one type of electrical load for another. (Answer 6).
2. Appellant does not separately address this issue. (Br. 13, and Reply Br.).
3. We find that the Examiner's reasoning for the modification of the load in Goluszek is supported by the prior art.

#### PRINCIPLES OF LAW

On appeal, Appellant bears the burden of showing that the Examiner has not established a legally sufficient basis for the rejection of the claims.

"In reviewing the [E]xaminer's decision on appeal, the Board must necessarily weigh all of the evidence and argument." *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).

It is axiomatic that anticipation of a claim under § 102 can be found only if the prior art reference discloses every element of the claim. See *In re King*, 801 F.2d 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1986) and *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1458, 221 USPQ 481, 485 (Fed. Cir. 1984).

Appellant has raised the issue of Goluszek teaching away from the claimed invention. Our guiding court has held "[t]he prior art's mere

disclosure of more than one alternative does not constitute a teaching away from any of these alternatives because such disclosure does not criticize, discredit, or otherwise discourage the solution claimed in the ‘198 application.’” *In re Fulton*, 391 F.3d 1195, 1201, 73 USPQ2d 1141, 1146 (Fed. Cir. 2004).

Our reviewing court states in *In re Zletz*, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989) that “claims must be interpreted as broadly as their terms reasonably allow.” Our reviewing court further states, “[t]he terms used in the claims bear a ‘heavy presumption’ that they mean what they say and have the ordinary meaning that would be attributed to those words by persons skilled in the relevant art.” *Texas Digital Sys. Inc v. Telegenix Inc.*, 308 F.3d 1193, 1202, 64 USPQ2d 1812, 1817 (Fed. Cir. 2002).

## ANALYSIS

Appellant has contended that Examiner erred in rejecting claims 1, 2, 4, 5, 7, 8, 14-22, 28-51, 53-55, and 57-62 under 35 U.S.C. §§ 102(b) and 103(a). Reviewing the findings of facts cited above, the recited elements of those claims are either anticipated by Goluszek or rendered obvious over his teaching, alone or in view of the teachings of Wang. Appellant’s arguments have been considered, but have not been found persuasive.

## CONCLUSION OF LAW

Based on the findings of facts and analysis above, we conclude that the Examiner did not err in rejecting claims 1, 2, 4, 5, 7, 8, 14-22, 28-51, 53-55, and 57-62.

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DECISION

The rejection of claims 1, 2, 4, 5, 7, 8, 14-22, 28-51, 53-55, and 57-62 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv)(2006).

AFFIRMED

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