

The opinion in support of the decision being entered today was *not* written for publication and is *not* binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte HONGJIANG SONG

Appeal 2007-0157
Application 10/984,584
Technology Center 2800

Decided: March 26, 2007

Before JOSEPH L. DIXON, HOWARD B. BLANKENSHIP,
and ALLEN R. MACDONALD, *Administrative Patent Judges*.
DIXON, *Administrative Patent Judge*.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the Examiner's final rejection of claims 1-4, 6-11, 15, 21, 22, 24-28, and 30. Claims 16-20 are indicated as allowable over the prior art and upon the filing of a Terminal Disclaimer. Claims 5, 12-14, 23, and 29 are objected to as depending from a rejected claim and would be allowable upon the filing of a Terminal Disclaimer.

We AFFIRM.

BACKGROUND

Appellant's invention relates to a buffer/voltage-mirror arrangement for sensitive node voltage connections. An understanding of the invention can be derived from a reading of exemplary claim 1, which is reproduced below.

1. A buffer circuit comprising:

an input stage comprising electrically-parallel branches of a first transistor connected in series with a second transistor, and a third transistor connected in series with a fourth transistor, said second and fourth transistors being of an inverse type to that of said first and third transistors, a gate interconnection electrically connecting gates of said first and second transistors to one another, and an intermediate electrical connection connecting all of the gates of said third and fourth transistors, an intermediate point between said first and second transistors and an intermediate point between said third and fourth transistors to one another, wherein said first and third transistors have width-to-length ratios which are substantially equal to one another, and said second and fourth transistors have width-to-length ratios which are substantially equal to one another;

an output stage comprising electrically-parallel branches of a first transistor connected in series with a second transistor,

and a third transistor connected in series with a fourth transistor, said second and fourth transistors being of an inverse type to that of said first and third transistors, a gate interconnection electrically connecting gates of said first and second transistors to one another, and an intermediate electrical connection connecting all of the gates of said third and fourth transistors, an intermediate point between said first and second transistors and an intermediate point between said third and fourth transistors to one another, wherein said first and third transistors have width-to-length ratios which are substantially equal to one another, and said second and fourth transistors have width-to-length ratios which are substantially equal to one another; and

wherein:

 said gate interconnection of said input stage is coupled to an input voltage;

 said intermediate electrical connection of said input stage is coupled to said gate interconnection of said output stage; and

 said intermediate electrical connection of said output stage is coupled to an output voltage that substantially mirrors said input voltage by a predetermined factor.

PRIOR ART

The prior art references of record relied upon by the Examiner in rejecting the appealed claims are:

Hsu	US 3,946,327	Mar. 23, 1976
Song	US 6,847,236 B1	Jan. 25, 2005

Hodges et al. (Hodges), *Analysis and Design of Digital Integrated Circuits*, McGraw-Hill Inc., 1988, 2nd edition, section 10.5.4, 408-409.

Appellant's Admitted Prior Art, Figure 1 (AAPA)

REJECTIONS

Claims 1-30 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 3, 6, 9, 16-19 of Song. Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 1-30 of Song meet all the limitations of claims 1-30 of the instant application.

Claims 1-4, 6-11, 21, and 22 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu in view of Hodges.

Claims 15, 24-28, and 30 stand rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Hsu and further in view of Hodges.

Rather than reiterate the conflicting viewpoints advanced by the Examiner and the Appellant regarding the above-noted rejections, we make reference to the Examiner's Answer (mailed Jul. 07, 2006) for the reasoning in support of the rejections, and to Appellant's Brief (filed Apr. 20, 2006) and Reply Brief (filed Sep. 11, 2006) for the arguments thereagainst.

OPINION

In reaching our decision in this appeal, we have given careful consideration to Appellant's specification and claims, to the applied prior art references, and to the respective positions articulated by Appellant and the Examiner. As a consequence of our review, we make the determinations that follow.

OBVIOUSNESS-TYPE DOUBLE PATENTING

Appellant has elected not to appeal this rejection by the Examiner therefore, we DISMISS Appellant's appeal with respect to claims 1-30 with respect to the obvious-type double patenting.¹

35 U.S.C. § 103

Initially, we note that Appellant has already obtained a patent on more narrowly claimed subject matter with specific fields of use recited in the preambles in the above Song patent. Here, Appellant seeks broader claimed subject matter reciting “a buffer,” “a method,” and “a system.”

Appellant’s main contention is that the Examiner did not “identify sufficient prior art evidence of a rationale for combining Hsu and Hodges” (Br. 16). We disagree with Appellant and find that the requisite showing by the Examiner is commensurate with the broad scope of Appellant’s instant claim language.

Appellant argues that “Hodges does not mention long-bus lines or large-capacitance downstream circuitry” as advanced by the Examiner as a motivation for combining the teachings of Hsu and Hodges. We do not find it a problem that the express words the Examiner used are not found in the text of the reference. The Examiner further discusses the rationale for the combination at page 7 of the Answer. We find no error in the Examiner’s reasoning for the combination or motivation.

¹ Here, we additionally question why the Examiner indicated claims allowable and also rejects all the claims based upon obvious-type double patenting. We leave it to the Examiner to clarify the status of the claims.

Appellant argues that:

The advantage discussed in Hodges accrues to a buffer in a digital circuit, not an analog amplifier such as shown by Hsu. The advantages of Hodges are irrelevant to the amplifier of Hsu because it is used in a different type of circuit. Also, the advantages of Hsu (providing a gain) are irrelevant to a buffer in a digital circuit which only switches between high and low

(Reply Br. 3). Here, we would agree with Appellant concerning a specific field of endeavor or circuit, but we do not find either recited in the instant claim language. Here, we find no specific field of endeavor or circuit in the language of independent claim 1. Considering the general teachings of Hsu and Hodges, we find that the general teachings are both applicable to both analog and digital circuits or a combination of them as in a sample and hold circuit where a digital value is sampled and held/buffered for digital processing by some further digital circuitry. Therefore, we do not find that the Examiner is completely baseless as Appellant contends, nor do we find that Hsu and Hodges expressly teach away from the combination as Appellant contends. We find that Appellant has not identified any specific language or teaching to support the contention that “both Hsu and Hodges teach away from the combination” (Br. 16).

Appellant argues that the Examiner has used Appellant’s disclosure as a road map to piece together the claimed invention from the prior art (Br. 16). We do not agree with Appellant. Appellant contends that the Examiner has not presented evidence of a reasonable expectation of success and analysis of the cascaded design of an amplifier (Br. 17). We find it within the level of skill in the art to cascade multiple amplifiers to compound their gain. The teachings of Hodges suggest having a circuit on the output which isolates the

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remainder of the circuit for external processing or influences/loads which we find suggestive in Hsu also as the Examiner advances.

Appellant argues that the instant application shows an analog circuit to mirror a voltage and that Hsu and Hodges are not analogous art (Reply Br. 2). We disagree with Appellant's argument since we do not find it commensurate in scope with the claimed invention. While Appellant's patented claims recite these types of limitations, we do not find that the instant claims support these arguments. Therefore, Appellant's argument is not persuasive.

Appellant argues the express language used by the Examiner in the discussion of Hodges concerning bus line and capacitance (Reply Br. 3). While we could speculate about a wealth of specific instances where the combination may not ring true, we find that there are instances where the general teachings and suggestions are combinable. Here, we find no specific field of endeavor to limit the combinability and find that it would have been obvious to one skilled in the art at the time of the invention to have looked to the teachings of Hodges with respect to having a input stage and output stage which are similar as recited in independent claim 1 and claims 2-4, 6-11, 21, and 22 grouped therewith by Appellant. Therefore, appellants' argument is not persuasive, and we will sustain the rejection of independent claim 1 and the claims grouped therewith.

With respect to dependent claim 15 and claims 24-28 and 30 grouped therewith, Appellant argues that Figure 1 AAPA only shows an environment for testing voltages, and that the motivation for combining Hsu and Hodges is not the same and not relevant (Br. 18). We disagree with Appellant and

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find that each motivation would be different for a different recited field of endeavor. Here, we only find a generic method in claim 15.

Here, we find sufficient motivation to combine the teachings of Hsu and Hodges and apply the combined teaching to the automatic test equipment field as taught by AAPA. With respect to Appellant's argument concerning a long bus/transmission line, we find this relative to the distances, voltages and capacitive values involved. In the instant claimed invention, we find little point of reference or context. Therefore, we find the Examiner's motivation not unreasonable or flawed as Appellant contends. Therefore, Appellant's argument is not persuasive, and we will sustain the rejection of claim 15 and claims 24-28 and 30.

CONCLUSION

To summarize, we have sustained the Examiner's rejection of claims 1-4, 6-11, 15, 21, 22, 24-28, and 30 under 35 U.S.C. § 103(a).

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No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

tdl/gw

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