

The opinion in support of the decision being entered today was *not* written for publication and is *not* binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SHINJI TOYOYAMA and YUICHI SATO

Appeal 2007-0803
Application 10/197,801
Technology Center 2800

Decided: May 15, 2007

Before JAMES D. THOMAS, LEE E. BARRETT, and MAHSHID D. SAADAT, *Administrative Patent Judges*.

THOMAS, *Administrative Patent Judge*.

DECISION ON APPEAL

This appeal involves claims 1, 5, 10 through 12, 14 through 17, and 21 through 25, Appellants having canceled claims 2 through 4, 6 through 9, 13, and 18 through 20. We have jurisdiction under 35 U.S.C. §§ 6(b) and 134(a).

Representative independent claim 1 is reproduced below as best representative of the disclosed and claimed invention:

1. A MOS transistor circuit comprising:

switching means for electrically switching a connection of a semiconductor substrate or well in which a first MOS transistor is formed to either a gate terminal of the first MOS transistor or a substrate voltage terminal for the semiconductor substrate or well, wherein the switching means comprises:

a switch having a second MOS transistor whose source and drain terminals are connected to the gate terminal and the semiconductor substrate or well of the first MOS transistor, respectively, and a third MOS transistor whose source and drain terminals are connected to the substrate voltage terminal and the semiconductor substrate or well of the first MOS transistor, respectively,

wherein the second MOS transistor or the third MOS transistor is an n-type MOS transistor and the other is a p-type MOS transistor, and when the first MOS transistor is in an active state, the second MOS transistor is turned on and the third MOS transistor is turned off to connect the semiconductor substrate or well to the gate terminal, and when the first MOS transistor is in a standby state, the second MOS transistor is turned off and the third MOS transistor is turned on to connect the semiconductor substrate or well to the substrate voltage terminal, and

wherein the gate terminals of the second MOS transistor and the third MOS transistor are electrically connected to each other in order to receive a switching signal for switching the first MOS transistor between the active and standby states,

wherein an absolute value of the threshold voltage of the first MOS transistor is set to be a lower value in the active state than in the standby state.

The following references are relied on by the Examiner:

Hirano	US 6,304,110 B1	Oct. 16, 2001 (filed October 27, 1998)
Mattison	US 5,179,295	Jan. 12, 1993

Pages 3 and 4 of the Answer identify all claims on appeal as rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 25 of U.S. Patent 6,469,568. Claims 1, 5, 10 through 12, and 14 through 17 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Hirano. On the other hand, claims 21 through 25 stand rejected under 35 U.S.C. § 103. As evidence of obviousness, the Examiner relies upon Mattison in view of Hirano.

Rather than repeat the positions of the Appellants and the Examiner, reference is made to the Brief and Reply Brief for the Appellants' positions, and to the Answer for the Examiner's positions.

OPINION

We affirm.

Turning first to the rejection of all claims on appeal under the judicially created doctrine of obviousness-type double patenting, since the remarks at the top of page 15 of the principal Brief on appeal indicate that a terminal disclaimer has not been filed in this application, we sustain this rejection. Correspondingly, this rejection has not been traversed on the merits.

In like manner, we have concluded that the Appellants have not set forth any arguments or evidence before us in the Brief and Reply Brief that the Examiner has erred in any manner as to the rejection of the identified claims under 35 U.S.C. §§ 102 and 103. Accordingly, we affirm these rejections as well.

Of independent claims 1 and 11 included within the rejection under 35 U.S.C. § 102, Appellants only present arguments to these independent claims collectively and present no separate arguments to the remaining dependent claims encompassed by this rejection. The arguments at pages 16 through 20 of the principal Brief on appeal focus only on the meaning to be attributed to the claimed “active state” and “standby state.” Appellants repeatedly present arguments to us that urge us to read so-called definitions of these states from the Specification into the claims such as the discussion at pages 13 through 15 of the Specification as filed. The position presented at the bottom of page 17 of the principal Brief on appeal, for example, that the artisan would interpret these stated states of representative independent claim 1 on appeal consistent with the present disclosure is noted. However, the reasoning advanced there and at the bottom of page 18 urging us that the skilled artisan “would be able to ascertain the intended definition of ‘active and standby states’ by reading the present specification, particularly on at least page 13, lines 7-12; and page 14, line 20 to page 15, line 17” invites us to read the significant discussion of these portions of the Specification into the claims which we decline to do. It appears that Appellants are more specifically inviting us to read the disclosed and unclaimed feature of a low threshold voltage having an increased on current and a high threshold voltage associated with a decreased off-current into the subject matter recited in the independent claims on appeal. Clearly, because these features are not recited in claims 1 and 11, the arguments are not persuasive of patentability.

Moreover, referring to the approach followed at pages 6 through 11 in the Answer, where the Examiner details the Examiner's responsive arguments to those positions set forth in the Brief, we agree with the Examiner's initial observation at page 6 that the subject matter of representative independent claim 1 on appeal essentially defines within its own terms the meaning to be attributed of the active and standby states claimed. The Examiner then goes into great detail persuasively explaining the correlations and functionalities of claimed features to the teachings and showings principally at columns 7 and 8 and the showing at figure 5 of Hirano. Significantly, the Examiner goes into great detail to explain the correlations of the teachings to claimed active and standby states. Equally significant as well is the Examiner's discussion beginning at page 8, which is again repeated through the discussion up to the top of page 10 of the Answer, that alternatively takes the position that the disclosed and intended meaning of the terminology, even though it is not recited in claim 1 on appeal, is also met by the Examiner's explanation.

It is equally important here to note that the subject matter recited in the wherein clause at the end of claim 1 on appeal reciting that "an absolute value of the threshold voltage of the first MOS transistor is set to be a lower value in the active state than in the standby state" is also directly addressed particularly by the Examiner's discussion at pages 9 and 10 of the Answer.

We also make note here the discussion at page 5 of the Specification as filed relating to acknowledged prior art at lines 11 through 19. This portion of the Specification indicates that it was known that an active state relates to a switching operation that is performed and a standby state relates to the switching operation that is not performed. Significantly as well, the

discussion at lines 16 through 18 states that “the absolute value of the threshold voltage of a MOS transistor is set to be low in the active state and high in the standby state,” as recited at the end of claim 1 on appeal.

Correspondingly, we are equally unpersuaded by Appellants’ remarks as to the rejection of the identified claims under 35 U.S.C. § 102 according to topics 1 through 4 discussed at pages 3 through 8 of the Reply Brief. Again, Appellants invite us to read into the claimed subject matter the Specification by asserting that the Examiner’s views with respect to an “active state” and “standby state” are not a “complete definition” of these states as urged at page 5 of the Reply Brief. To the extent pages 4 and 5 of the Reply Brief urge the Examiner has improperly relied upon inherency with respect to Hirano, the Examiner has not formally recited any inherency argument except the discussion at page 11 of the Answer. There, the Examiner merely uses the term inherency to describe what Hirano explicitly teaches was known in the prior art as depicted in his figures 12 and 13 which the Examiner directly correlates to be consistent with Appellants’ own disclosed recognition of the inherent operation of the claimed transistors. It appears to us that to the extent Appellants are arguing the inherency of the claimed invention based upon their own disclosure, a rather unique argument in itself, the Examiner is certainly permitted to take the positions taken at page 11 of the Answer since Hirano specifically teaches about the known properties of the identified transistors, which is consistent with Appellants’ own disclosed characterization of these same transistors.

Pages 7 and 8 of the Reply Brief improperly make reference to Hirano's alleged failure to consider the problem solved by Appellants' present invention. Notwithstanding the fact that representative independent claim 1 on appeal does not recite a circuit which can increase on-current and reduce off-current in an active state and further reduce the off-current in a standby state, such problem-to-be-solved approach is not proper within a rejection under 35 U.S.C. § 102.

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. *See In re Fine*, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the Examiner must make the factual determinations set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 17, 148 USPQ 459, 467 (1966). Furthermore, “there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness’ [H]owever, the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.” *KSR Int’l Co. v. Teleflex Inc.*, No. 04-1350, slip op. at 14 (U.S., Apr. 30, 2007)(quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)). In this appeal, we are satisfied the examiner has met the requirements of the recent precedent, as embellished upon here.

As to the rejection of claims 21 through 25 under 35 U.S.C § 103 as being obvious over Mattison in view of Hirano, we are unpersuaded by the corresponding arguments beginning at page 20 of the principal Brief on appeal as to these claims. The arguments presented here do not contest the proper combinability of these references within 35 U.S.C. § 103 to meet the

subject matter of the claims of rejected claims. Correspondingly, to the extent pages 8 and 9 of the Reply Brief attempt to argue that it would not have been obvious to have combined these references, that there is no motivation to modify Hirano or that there is improper hindsight exercised by the Examiner, the arguments are not considered since they were presented in a untimely manner in a Reply Brief and not first presented in a timely manner in the principal Brief on appeal. In context as well, the positions set forth at pages 8 and 9 of the Reply Brief appear to only apply to the master-slave flip-flop feature recited only in the preamble of independent claim 23 on appeal.

The other remarks at page 22 of the Reply Brief relating to the rejection under 103 argues features associated with Hirano that have been dealt with, with respect to our earlier discussion of the rejection of other claims under Section 102. Pages 5 and 6 of the Answer set forth a view that it was notoriously well known in the art to connect two latches in cascade to construct a master-slave flip flop as applied to claims 23 and 24 on appeal. This view is only briefly and generally mentioned at the bottom of page 22 of the principal Brief on appeal. The Examiner's Responsive arguments at pages 11 and 12 in the Answer as to these arguments of this rejection distinguish between the Examiner's views as to independent claims 21, 22, and 25 on appeal and the Examiner's views with respect to independent claim 23 and its dependent claim 24 on appeal. The remarks at page 8 and 9 of the Reply Brief do not contest the Examiner's views expressed as to the notoriousness of this position of the Examiner and make no mention that the Examiner has well documented at page 12 of the Answer that a previously

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cited reference of record in this application but not applied in the rejection does illustrate this relationship of a master-slave combination of flip flops.

In summary, we have affirmed the Examiner's rejection of all claims on appeal under the judicially created doctrine of obviousness-type double patenting. Likewise, based upon the weight and extent of the Examiner's arguments and evidence of unpatentability of the respectively rejected claims under 35 U.S.C. §§ 102 and 103, the rejections of these claims, which encompass all claims on appeal, are affirmed. Therefore, the decision of the Examiner is affirmed.

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No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. §1.136(a). See 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

PGC

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