

The opinion in support of the decision being entered today is *not* binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SILVIO E. BOU-GHAZALE, CUONG M. LE,
MICHAEL S. JONES, and TIMOTHY J. FISHER

Appeal 2007-0842
Application 09/789,196
Technology Center 2800

Decided: July 11, 2007

Before JAMES D. THOMAS, HOWARD B. BLANKENSHIP, and
JEAN R. HOMERE, *Administrative Patent Judges*.

HOMERE, *Administrative Patent Judge*.

DECISION ON APPEAL
STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134 from the Examiner's Final Rejection of claims 1 through 5, 7, 11 through 15, 17, 21 through 25, and 27. We have jurisdiction under 35 U.S.C. § 6(b) to decide this appeal.

Appellants invented a method and system for modeling blocks of an integrated circuit (IC) for timing verification. Particularly, the invention performs a block-level static timing analysis that allows exception paths and multi-cycle paths to be specified at the block boundaries. (Specification 2).

Claim 1 is illustrative of the claimed invention. It reads as follows:

1. A method comprising:

receiving block electrical connectivity information for a plurality of block pins, at least one of said block pins being coupled to one or more sequential elements;

identifying the first sequential element coupled to said at least one block pin; and

developing block model including said first sequential element and the combinational logic between said element and said at least one block pin.

In rejecting the claims on appeal, the Examiner relied upon the following prior art:

Segal

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Dec. 17, 2002

The Examiner rejected the claims on appeal as follows:

Claims 1 through 5, 7, 11 through 15, 17, 21 through 25, and 27 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Segal.

Appellants contend¹ that Segal does not anticipate the cited claims. Particularly, Appellants contend that Segal does not fairly teach or suggest developing a block model having a combinational logic located between a sequential element and a block pin, as recited in independent claims 1, 11, and 21. (Br. 7; Reply Br. 3). Further, Appellants contend that Segal does not teach each and every limitation of claims 2 through 5, 7, 12 through 14, 17, 25 through 27. In response, the Examiner contends that Segal teaches the cited limitations, and therefore anticipated claims 1 through 5, 7, 11 through 15, 17, 21 through 25, and 27. (Answer² 7 through 12.)

We affirm.

ISSUES

The *pivotal* issue in the appeal before us is as follows:

Have Appellants shown that the Examiner failed to establish that the disclosure of Segal anticipates the claimed invention under 35 U.S.C. § 102(b)? More particularly, does Segal's disclosure teach a block model that includes a combinational logic located between a first sequential element and a block pin?

¹ This decision considers only those arguments that Appellants submitted in the Appeal and Reply Briefs. Arguments that Appellants could have made but chose not to make in the Briefs are deemed to have been waived. *See* 37 C.F.R. § 41.37(c)(1) (vii)(eff. Sept. 13, 2004). *See also In re_Watts*, 354 F.3d 1362, 1368, 69 USPQ2d 1453, 1458 (Fed. Cir. 2004).

² We rely on and refer to the Supplemental Examiner's Answer mailed on May 22, 2006.

FINDINGS OF FACT

The following findings of fact are supported by a preponderance of the evidence.

The Invention

1. Appellants invented a method and system for modeling blocks of an IC (10) for timing verification by performing a block-level static timing analysis allowing exception paths and multi-cycle paths to be specified at the block boundaries (Specification 2).

2. As depicted in Figure 1, the IC (10) is divided into a plurality of functional blocks (12a, 12b, 12c). (*Id.* 4.)

3. As depicted in Figure 2, each functional block (12c) includes a plurality of block pins (13), sequential elements (18), and combinational logic (14, 16). (*Id.* 5)³

4. One or more block pins (13) are coupled to one or more sequential elements (18) to develop a block model, which includes electrical paths between the block pins. Particularly, the electrical paths are formed by placing the combinational logic (14, 16) between the sequential element (18) and the block pin (13). (*Id.*)

5. The developed model further excludes exception paths with a combinational logic that is not located between the sequential element and the block pin. (*Id.* 5)

³ Appellants' Specification, at page 3, provides the following definitions:
A block pin is the connection to a boundary of the block. It connects the block to the exterior of the block.
Combinational logic is any circuit element whose output is not dependent on a clock or reference signal.
A sequential element is any circuit element that captures, samples or stores at least one data signal based on another reference signal such as a clock.

The Prior Art Relied upon

6. Segal teaches a method and system for optimizing functional blocks of an IC (301) by utilizing models to perform static timing analysis for each block of the circuit. (Abstract; col. 11, ll. 55-58.)

7. As depicted in Figure 3A, Segal teaches dividing the IC (301) into a plurality of functional blocks (302 through 305) with corresponding timing constraints and exceptions to optimize the circuit (301). (Col. 11, ll. 19-25; col. 12, ll. 9-22.)

8. Segal teaches creating models to replace each of the functional blocks to calculate timing constraints and exceptions to optimize the circuit. (Col. 11, ll. 28-34; col. 12, ll. 52-58, Figure 11B.)

9. Segal teaches adding information at the model pins (X,Y) to represent parts of the exception paths that are eliminated from the model, but present in the circuit block. (Col. 17, ll. 15-18.)

10. Segal teaches choosing boundaries between circuit blocks by using input/output pins of the model boundary. (Col. 15, ll. 22-27; col. 16, ll. 17-19.)

11. As depicted in Figure 7, Segal teaches a circuit block (302) having an AND gate (B), which is fed by a sequential element (A) and another AND gate (C). Blocks 302 and 303 are connected externally at point D. (Answer 7-8.)

12. As depicted in Figure 12A, Segal teaches a plurality of serially coupled gates (1115-1115d) located between sequential circuits (1120a-1120b). (Col. 17, ll. 33-36.)

13. Segal teaches a “create_clock” command in the model definition to generate a virtual clock, which is used to define start and end points in static timing analysis. (Col. 29, ll. 1-20.)

PRINCIPLES OF LAW
ANTICIPATION

It is axiomatic that anticipation of a claim under § 102 can be found only if the prior art reference discloses every element of the claim. *See In re King*, 801 F.2d 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1986) and *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1458, 221 USPQ 481, 485 (Fed. Cir. 1984).

In rejecting claims under 35 U.S.C. § 102, a single prior art reference that discloses, either expressly or inherently, each limitation of a claim invalidates that claim by anticipation. *Perricone v. Medicis Pharmaceutical Corp.*, 432 F.3d 1368, 1375-76, 77 USPQ2d 1321, 1325-26 (Fed. Cir. 2005), citing *Minn. Mining & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc.*, 976 F.2d 1559, 1565, 24 USPQ2d 1321, 1326 (Fed. Cir. 1992). Anticipation of a patent claim requires a finding that the claim at issue “reads on” a prior art reference. *Atlas Powder Co. v. IRECO, Inc.*, 190 F.3d 1342, 1346, 51 USPQ2d 1943, 1945 (Fed. Cir. 1999) (“In other words, if granting patent protection on the disputed claim would allow the patentee to exclude the public from practicing the prior art, then that claim is anticipated, regardless of whether it also covers subject matter not in the prior art.”) (internal citations omitted).

ANALYSIS

As set forth above, independent claims 1, 11, and 21 require developing a block model having a combinational logic located between a sequential element and a block pin. In our view, Segal reasonably discloses such development of a block model. In reaching this conclusion, we construe the terms combinational logic, sequential element, and block pin, as per the definitions provided in Appellants' Specification.⁴ As detailed in the Findings of Fact section above, Segal discloses creating a model for each circuit block. (Finding of Fact 8.) Further, Segal discloses a circuit block having an AND gate (C), the output of which is not dependent upon the input/output of the sequential element (A). Therefore, the AND gate (C) meets Appellants' definition for the claimed combinational element. Similarly, point D meets the definition for the claimed block pin since point D connects the exterior of blocks 302 and 303. Additionally, Segal teaches choosing boundaries between circuit blocks by using input/output pins of the model boundary. (Finding of Facts 9 and 10.) Therefore, the Examiner's reliance on Segal's model to teach the claimed block model comports with the broadest reasonable interpretation of these terms as would be understood by an ordinarily skilled artisan. In light of these findings, it is our view that

⁴ See *supra* note 3. Application claims are interpreted as broadly as is reasonable and consistent with the specification, "taking into account whatever enlightenment by way of definitions or otherwise that may be afforded by the written description contained in the applicant's specification." *In re Morris*, 127 F.3d 1048, 1054, 44 USPQ2d 1023, 1027 (Fed. Cir. 1997). A definition can be explicit or implicit. See *Massachusetts Institute of Technology v. Abacus Software*, 462 F.3d 1344, 1351, 80 USPQ2d 1225, 1229 (Fed. Cir. 2006) ("the specification does not define the term 'scanner' either explicitly or implicitly").

Segal teaches the cited limitations of independent claims 1, 11, and 21. It follows that the Examiner did not err in rejecting claims 1, 11, and 21 as being anticipated by Segal.

With regard to the rejection of dependent claims 2 through 5, 7, 12 through 15, 17, 22 through 25, and 27, we are in general agreement with the Examiner for the reasons set forth in the Answer. We find that Appellants' arguments are not persuasive. They fail to particularly show any error in the Examiner's rejection. Instead, Appellants' arguments summarily allege that Segal does not, in every instance, teach the limitation of each of the cited claims. Since Appellants have not provided us with adequate evidence to show error in the Examiner's rejection of these dependent claims, we sustain the Examiner's rejection for the reasons set forth in the Answer.

CONCLUSIONS OF LAW

On the record before us, Appellants have not shown that the Examiner failed to establish that Segal anticipates claims 1 through 5, 7, 11 through 15, 17, 21 through 25, and 27 under 35 U.S.C. § 102(e).

OTHER ISSUES

The Examiner may reconsider whether claims 1 through 10 should be rejected under 35 U.S.C. § 101, as not being directed to statutory subject matter. The claims recite a method that appears directed to the abstract idea of developing a block model.⁵

⁵ A case involving similar issues (*Ex parte Bilski*, S.N. 08/833,892, Appeal No. 2002-2257) is presently on appeal at the Federal Circuit. The Board's opinion, available at <http://www.uspto.gov/web/offices/dcom/bpai/its/fd022257.pdf>, is designated an "Informative Opinion" of the Board.

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DECISION

We have affirmed the Examiner's decision rejecting claims 1 through 5, 7, 11 through 15, 17, 21 through 25, and 27.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a) (1) (iv).

AFFIRMED

gw

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