UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte RICHARD SCOTT LIST,
BRUCE A. BLOCK
and RUITAO ZHANG

Appeal 2007-0898
Application 09/962,786
Technology Center 2800

Decided: March 7, 2007

Before EDWARD C. KIMLIN, CHUNG K. PAK, and JEFFREY T. SMITH, *Administrative Patent Judges*.

KIMLIN, *Administrative Patent Judge*.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1, 2, 4, 6, and 8-10. Claims 11-23 have been withdrawn from consideration. Claim 1 is illustrative:

1. A method comprising:

providing an integrated circuit having a layer of meal;

forming an on-chip decoupling capacitor stack, the on-chip decoupling capacitor stack including,

a bottom electrode on the layer of metal;

a dielectric layer;

a top electrode separated from the bottom electrode by the dielectric layer; and

a conductive top electrode barrier contacting the top electrode,

wherein the top electrode barrier comprises a material that is more electrically conductive than a material for the top electrode, and

wherein the top capacitor electrode is formed on the dielectric layer and the top electrode barrier is formed on the top electrode in a single deposition chamber without removing the on-chip decoupling capacitor stack from the single deposition chamber.

The Examiner relies upon the references as evidence of obviousness:

Kirlin	US 5,976,928	Nov. 2, 1999
Kang	US 6,180,482 B1	Jan. 30, 2001
Nozaki	US 6,389,754 B2	May 21, 2002

Sze, "Physics of Semiconductor Devices," Second Edition, John Wiley & Sons, Appendix 1, p. 852 (1981).

Shimada, "Tantalum Nitride Metal Gate FD-SOI CMOS FETs Using Low Resistivity Self-Grown bcc- Tantalum Layer, "IEEE trans. on Electron Device, 48, (Aug. 2001) 1619-1626.

The Appellants' claimed invention is directed to a method of making on-chip integrated circuit decoupling capacitors that, according to Appellants, may serve to prevent voltage drop on the power grid for high surge current conditions. The method entails, inter alia, forming a top electrode barrier on the top electrode with the provision that the top electrode comprises a material that is more electrically conductive than the material of the top electrode. For example, the top electrode barrier may be Ta whereas the top electrode may be TaN.

Appealed claims 1, 2 and 4 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dalton in view of Shimada. Claims 6, 8, and 10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the stated combination of references further in view of Kirlin and Sze. In addition, claim 9 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Dalton in view of Shirmada, Kirlin, Sze, and Kang.

We have thoroughly reviewed the respective positions advanced by Appellants and the Examiner. In so doing, we find ourselves in agreement with Appellants that the Examiner has failed to establish a prima facie case of obviousness for the claimed method. Accordingly, we will not sustain the Examiner's rejections.

The Examiner appreciates that Dalton fails to teach the presently claimed top electrode barrier layer. Hence, the Examiner applies Shimada for evidencing the obviousness of including a top electrode barrier layer on the top electrode of Dalton. However, as emphasized by Appellants, Shimada fails to teach that the top electrode barrier material is one that is more electrically conductive than the material of the top electrode, as

presently claimed. In particular, Shimada specifically discloses a barrier layer of TaN over a top electrode of Ta, which results in a relative conductivity exactly the opposite of that claimed.

The Examiner points out that Shimada discloses a stack for a MOS capacitor with a Ta layer grown on a TaN layer and concludes that the "Ta layer serves as a conductive barrier layer" (page 9 of Answer, third para.). However, as explained by Appellants, Shimada uses this structure without a barrier layer only to identify the crystal structure of the Ta layer. The Examiner has not explained why this disclosure would have motivated one of ordinary skill in the art to use a barrier layer of Ta on the top electrode of Dalton, and such requisite motivation is not apparent to us.

As for Kirlin, the Examiner has not refuted Appellants' argument that Kirlin, while disclosing a Ta barrier layer, uses Ta over a more electrically conductive top electrode 34, such as a noble metal.

In conclusion, based on the foregoing, we are constrained to reverse the Examiner's rejections.

REVERSED

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