

The opinion in support of the decision being entered today was *not* written for publication and is *not* binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte FARID NEMATI, KAILASH GOPALAKRISHNAN, and
ANDREW E. HORCH

Appeal 2007-0938
Application 10/706,162
Technology Center 2800

Decided: April 19, 2007

Before JOSEPH F. RUGGIERO, HOWARD B. BLANKENSHIP, and
JOHN A. JEFFERY, *Administrative Patent Judges*.

JEFFERY, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellants appeal under 35 U.S.C. § 134 from the Examiner's rejection of claims 1-6, 15, 19-22, 24, and 26. Claims 7-14, 16-18, 23, 25, and 27 have been indicated as containing allowable subject matter.¹ We have jurisdiction under 35 U.S.C. § 6(b).

STATEMENT OF THE CASE

Appellants invented a semiconductor device including a thyristor that overcomes problems associated with temperature-related effects on the device. In one embodiment, the thyristor has immediately adjacent base regions with first and second control ports. The first control port capacitively couples a first signal to one of the base regions to control current flow in the thyristor. A control circuit applies a DC voltage to the second control port as a function of temperature. Accordingly, bipolar gains in the thyristor are controlled for managing holding current and forward blocking voltage at a variety of temperatures.² Claim 1 is illustrative:

1. A semiconductor device comprising:
a thyristor having thyristor body regions including first and second immediately adjacent base regions between first and second emitter regions;

¹ A discrepancy exists in the Appeal Brief and the Answer regarding the objected claims. Appellants indicate that claims 4, 7, 16-18, 23, 25, and 27 are objected to (Br. 3), but the Examiner indicates that claim 4 is not objected to since it was also rejected (Answer 3). The Examiner's correction to the record regarding claim 4 is undisputed; we therefore presume that claim 4 was intended to be rejected.

Also, although neither the Briefs nor the Answer indicate the status of claims 11-14, these claims were also objected to as containing allowable subject matter. *See* Final Rejection 2 (indicating claims 7-14, 16-18, 23, 25, and 27 as objected to).

² *See generally* Specification 3-4.

a first control port configured and arranged to capacitively couple a first signal at least to the first base region; and
a second control port configured and arranged for receiving a second signal generated outside of the thyristor and for coupling the second signal at least to the second base region, the second signal being adapted to control holding current or forward blocking voltage of the thyristor as a function of temperature.

The Examiner relies on the following prior art reference to show unpatentability:

Nemati US 6,462,359 B1 Oct. 8, 2002

The Examiner's rejection is as follows:

Claims 1-6, 15, 19-22, 24, and 26 are rejected under 35 U.S.C. § 102(b) as being anticipated by, or, in the alternative, under 35 U.S.C. § 103(a) as obvious over Nemati.

Rather than repeat the arguments of Appellants or the Examiner, we refer to the Briefs³ and the Answer for their respective details. In this decision, we have considered only those arguments actually made by Appellants. Arguments which Appellants could have made but chose not to make in the Briefs have not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii).

OPINION

It is our view, after consideration of the record before us, that the disclosure of Nemati fully meets the invention set forth in claims 1, 2, 4-6,

³ Appellants filed an Appeal Brief on Oct. 21, 2005 which was amended by two amendments filed Mar 3, 2006 and Apr. 24, 2006 respectively. A Reply Brief was also filed Oct. 2, 2006.

15, 19-22, 24, and 26. We reach the opposite conclusion, however, with respect to claims 3-5. Moreover, we conclude that the evidence relied upon and the level of skill in the particular art would not have suggested to one of ordinary skill in the art the invention set forth in claims 3-5. Accordingly, we affirm-in-part.

Anticipation is established only when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of a claimed invention as well as disclosing structure which is capable of performing the recited functional limitations. *RCA Corp. v. Applied Digital Data Systems, Inc.*, 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir. 1984); *W.L. Gore and Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1554, 220 USPQ 303, 313 (Fed. Cir. 1983).

In addition, in rejecting claims under 35 U.S.C. § 103, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. *See In re Fine*, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the Examiner must make the factual determinations set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 17, 148 USPQ 459, 467 (1966). If that burden is met, the burden then shifts to the Appellants to overcome the prima facie case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole and the relative persuasiveness of the arguments. *See In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).

The Examiner has indicated how the claimed invention is deemed to be fully met by the disclosure of Nemati “or at least obvious depending on one’s interpretation of the ‘functional language’ in the claim” (Answer 4-5).

Regarding independent claim 1,⁴ Appellants argue that the claim requires that the second signal should be (1) generated outside of the thyristor, and (2) coupled to at least the second base region (Reply Br. 2).

According to Appellants, the external signal relied upon by the Examiner is not coupled to the base region of the thyristor. Appellants note that the gate of NMOSFET 850 in Fig. 8 of Nemati is coupled to the thyristor; therefore, the gate signal is not externally provided. Appellants further argue that even if the gate signal could be externally provided, it is used to control the resistance between the source and drain of the NMOSFET. Such a function, according to Appellants, is significantly different from coupling the signal to at least the second base region of the thyristor as claimed (Br. 5-6).

The Examiner argues that since the NMOSFET is directly coupled to the second base region (n Base) 814, the gate signal is therefore “coupled” to the second base region through the source/drain contact. The Examiner further notes that the gate of the NMOSFET can be independently controlled rather than being connected to the p Base as shown in Fig. 8 (Answer 6-7).

Appellants also argue that Nemati does not disclose an external signal for controlling the holding current or forward block voltage as a function of temperature. Rather, the gate-to-source voltage in Nemati varies with the state of the thyristor (i.e., the thyristor’s forward conducting versus forward blocking states) (Br. 6).

We will sustain the Examiner’s rejection of independent claim 1. At the outset, we note that claim 1 merely calls for a semiconductor device

⁴ Appellants indicate that claim 1 is representative of the group comprising claims 1, 2, 6, 15, 19-22, 24, and 26 (Br. 4).

comprising a thyristor and two control ports. Significantly, the first and second signals are merely *intended inputs* to the control ports, but otherwise do not further limit the structure of the semiconductor device itself. In short, the limitation in the last two lines of claim 1 calling for “the second signal being adapted to control holding current for forward blocking voltage of the thyristor as a function of temperature” merely pertains to the intended use of the device – not the device itself.

With this interpretation, we turn to Nemati. First, we see no reason why the identified second control port would not be capable of (1) receiving a second signal generated outside of the thyristor, and (2) coupling the second signal to the second base region, particularly in view of Nemati’s teaching that the gate of NMOSFET can be independently controlled rather than being connected to the p-base (Nemati, col. 7, ll. 35-37). The scope and breadth of the claim language simply does not preclude the identified second control port of Nemati that is capable of (1) receiving a signal generated outside of the thyristor, and (2) coupling the received signal to at least the second base region as claimed.

Because we find that Nemati anticipates representative claim 1, we will sustain the Examiner’s rejection of that claim. Since Appellants have not separately argued the patentability of claims 2, 4-6, 15, 19-22, 24, and 26 with particularity, these claims fall with representative claim 1.⁵ *See In re*

⁵ Although Appellants nominally argue the limitations of claim 6 for the first time in the Reply Brief (Reply Br. 4), we consider this argument waived because it was not raised in Appellants’ opening brief. *See Optivus Tech., Inc. v. Ion Beam Applications S.A.*, 469 F.3d 978, 989, 80 USPQ2d 1839, 1847-48 (Fed. Cir. 2006) (“[A]n issue not raised by an appellant in its opening brief...is waived.”) (internal citations and quotation marks omitted).

Nielson, 816 F.2d 1567, 1572, 2 USPQ2d 1525, 1528 (Fed. Cir. 1987); *see also* 37 C.F.R. § 41.37(c)(1)(vii).

We will not, however, sustain the Examiner's rejection of claims 3-5. We agree with Appellants that Nemati fails to teach or suggest a temperature sensing circuit, let alone a temperature sensing circuit configured and arranged to apply the second signal to the second control port as a function of the thyristor's temperature or increase bipolar gains of the thyristor when the thyristor's temperature is below a selected threshold as claimed.

The Examiner asserts that the NMOSFET 850 in Nemati constitutes the claimed temperature sensing circuit since it "provides temperature stability" (Answer 3, 8). However, the Examiner has not identified – nor can we find – any specific teaching or suggestion on this record that the NMOSFET senses temperature at all, let alone that it is configured and arranged to apply the second signal to the second control port responsive to the thyristor's temperature as claimed.

Although Nemati indicates that the current shunt, among other things, improves stability under high temperature conditions (Nemati, col. 2, ll. 60-65; col. 7, ll. 33-35), such a generally-stated benefit hardly suggests including a temperature sensing circuit as claimed. Rather, Nemati's NMOSFET shunts current responsive to the forward conducting or blocking state of the thyristor. That is, when the thyristor is in a forward conducting state, the voltage difference between the NMOSFET's gate and source is relatively small; thus, the NMOSFET passes only a small current. But the NMOSFET strongly shunts current when the thyristor is in a forward blocking state since the voltage difference between the NMOSFET's gate and source is very high (Nemati, col. 7, ll. 20-31).

The clear import of this teaching is that the NMOSFET is switched -- and current shunted -- solely in response to the forward conducting or blocking state of the thyristor. Merely because this technique ultimately provides high temperature stability does not, without more, reasonably suggest providing a temperature sensing circuit as claimed.

Furthermore, we acknowledge Nemati's alternative technique of independently controlling the gate of the NMOSFET instead of connecting the gate to the p Base (Nemati, col. 7, ll. 35-37). But the reference is silent regarding the specifics of this independent control, let alone that the control is associated with a temperature sensing circuit as claimed.

For at least these reasons, we conclude that Nemati neither anticipates nor renders obvious to the skilled artisan the subject matter recited in claims 3-5. Accordingly, we will not sustain the Examiner's rejection of those claims.⁶

⁶ As an ancillary observation, we note that no antecedent basis exists for "*the temperature sensing circuit*" in claim 4 (emphasis added). Because the parties did not raise this issue on appeal, it is not before us. In an *ex parte* appeal, "the Board is basically a board of review -- we review...rejections made by patent examiners." *Ex parte Gambogi*, 62 USPQ2d 1209, 1211 (BPAI 2001). Accordingly, we leave resolution of this issue to the Examiner and the Appellants.

DECISION

We have sustained the Examiner's rejection with respect to claims 1, 2, 4-6, 15, 19-22, 24, and 26. We have not, however, sustained the Examiner's rejections with respect to claims 3-5. Therefore, the Examiner's decision rejecting claims 1-6, 15, 19-22, 24, and 26 is affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

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AFFIRMED-IN-PART

ELD

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