

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KOJI SUZUKI

Appeal 2007-0995
Application 10/396,811¹
Technology Center 2800

Decided: May 29, 2008

Before JAMESON LEE, RICHARD TORCZON and SALLY C. MEDLEY,
Administrative Patent Judges.

MEDLEY, *Administrative Patent Judge.*

DECISION ON APPEAL

¹ Application for patent filed 26 March 2003.
The real party in interest is Oki Electric Industry Co., Ltd.

A. Statement of the Case

This is an appeal under 35 U.S.C. § 134 from the Examiner's Final Rejection of claims 5-7². We have jurisdiction under 35 U.S.C. § 6(b). We affirm.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Yokosawa 5,528,182 Jun. 18, 1996

Claims 5-7 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Yokosawa.

BACKGROUND

The invention is related to a power-on reset circuit. Referring to figure 2, the power-on reset circuit includes a first transistor circuit comprising first transistors PMOS **1** and NMOS **2** connected between first and second potentials **V_{DD}** and **GND**, a second transistor circuit comprising second transistors PMOS **3** and NMOS **4**, having an on resistance which is smaller than that of the first transistors, and a resistor **5** serially connected to the second transistors PMOS **3** and NMOS **4**, said second transistors and the resistor being also connected between the first and second potentials **V_{DD}** and **GND**. A first current flows to first transistors PMOS **1** and NMOS **2** and a second current flows to second transistors PMOS **3** and NMOS **4** and resistor **5** dependent on a voltage between the potentials **V_{DD}** and **GND**. An output circuit comprising NMOSs **6** and **7** and PMOSs **8** and **9** and an inverter **10** outputs a reset signal **POR** when the first current is greater than

² Claims 1-4 were allowed in the Advisory Action mailed 12 Nov. 2004. Claims 8-13 were objected to as being dependent upon a rejected base claim in the Advisory Action mailed 18 March 2005. Claims 14-20 were allowed in the Examiners Answer mailed 20 April 2005.

the second current upon comparison between the first and second currents.
(Spec. 4-8, **fig. 2**).

Figure 2 from the Application is reproduced below.

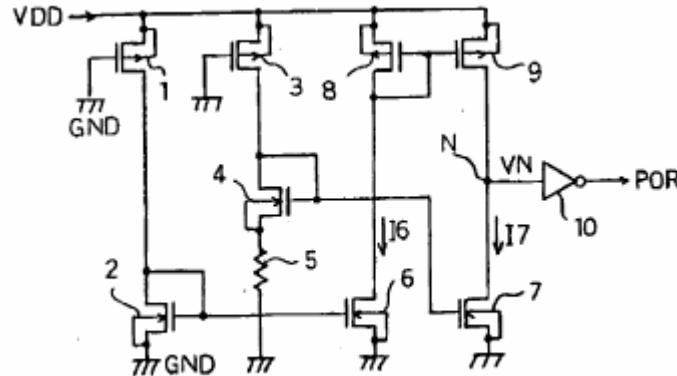


Figure 2 depicts a first transistor circuit, a second transistor circuit, a resistor, an output circuit and an inverter.

B. Issue

The issue before us is whether the Applicant has shown that the Examiner erred in finding that claims 5-7 are anticipated under 35 U.S.C. § 102(b) by Yokosawa. For the reasons that follow, the Applicant has failed to show that the Examiner erred in finding that claims 5-7 are anticipated under 35 U.S.C.

§ 102(b) by Yokosawa.

C. Findings of Facts (“FF”)

The record supports the following findings of facts as well as any other findings of fact set forth in this opinion by at least a preponderance of the evidence.

1. Applicant's claims 5-7 are the subject of this appeal.
2. Claim 5 is independent.
3. Claims 6-7 are dependent on claim 5.

4. Claims 5-7 stand or fall together (App. Br.³ 9).

5. Claim 5 is representative and is as follows:

A power-on reset circuit comprising:

a first current generation circuit connected between first and second potential sources, the first current generation circuit providing a first current therethrough;

a second current generation circuit connected between the first and second potential sources, the second current generation circuit providing a second current therethrough; and

a current comparison circuit coupled to the first and second current generation circuits, the current comparison circuit having an output node and comparing the first and second currents so as to provide a voltage at the output node based on the current comparison.

6. The Examiner found that Yokosawa describes a first current generation circuit **T1**, **T2**, **T3**, **T4** and **T8** and a second current generation circuit **T6**, **T7** and **T9** both connected between first and second potential sources **1** and **2**; the first current generation circuit providing a first current **It4** and the second current generation circuit providing a second current **I4**, and a current comparison circuit **Nc** and **C2** coupled to the first and second current generation circuits and an output node **Nc** and comparing the first and second currents so as to provide a voltage at the output node based on the current comparison (Ans. 4⁴ and Yokosawa fig. 3).

³ The Appeal Brief referred to hereinafter is the Supplemented Appeal Brief filed 26 Oct. 2006.

⁴ The rejection of claims 5-7 in the Examiner's Answer appears to be based on a different interpretation of Yokosawa than the interpretation utilized in the Final Rejection. Applicant addressed this interpretation in its Reply Brief.

7. Yokosawa describes that the potential **Vc** at the node **Nc** is determined in accordance with the values of the current driving capability **It4** of P-channel FET **T4** and the current driving capability **I4** of N-channel FET **T9** (Yokosawa col. 5, ll. 1-4).
8. Yokosawa describes **I4** as the current driving capability of the N-channel FET **T9** (col. 5, ll. 1-4).
9. Yokosawa describes **It4** as the current driving capability of the P-channel FET **T4** (col. 5, ll. 1-4).
10. Yokosawa describes **I4** as the current flowing into N-channel FET **T9** (col. 4, ll. 35-37).
11. Yokosawa describes that if **It4 < I4**, the potential **Vc** at node **Nc** becomes a low level and if **It4 > I4**, the potential **Vc** at node **Nc** becomes a high level (Yokosawa col. 5, ll. 5-15).

D. Principles of Law

“Anticipation under 35 U.S.C. § 102([b]) requires that ‘each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.’” *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999) (quoting *Verdegaal Bros., Inc. v. Union Oil Co.*, 814 F.2d 628, 631 (Fed. Cir. 1987)).

“In the patentability context, claims are to be given their broadest reasonable interpretations” and “limitations are not to be read into the claims from the specification.” *In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993).

Argument of counsel cannot take the place of evidence lacking in the record. *Meitzner v. Mindick*, 549 F.2d 775, 782 (CCPA 1977); *see also In re Pearson*, 494 F.2d 1399, 1405 (CCPA 1974).

E. Analysis

Claims 5-7 stand or fall together (FF⁵ 4). We focus our analysis on independent claim 5 which recites the limitation “a current comparison circuit . . . comparing the first and second currents so as to provide a voltage at the output node based on the current comparison.”

The Examiner found that Yokosawa describes a first current generation circuit **T1**, **T2**, **T3**, **T4** and **T8** and a second current generation circuit **T6**, **T7** and **T9** both connected between first and second potential sources **1** and **2**; the first current generation circuit providing a first current **It4** and the second current generation circuit providing a second current **I4**, and a current comparison circuit **Nc** and **C2** coupled to the first and second current generation circuits with an output node **Nc** for comparing the first and second currents so as to provide a voltage at the output node based on the current comparison (FF 6).

⁵ FF denotes Finding of Fact.

Figure 3 from Yokosawa is reproduced below.

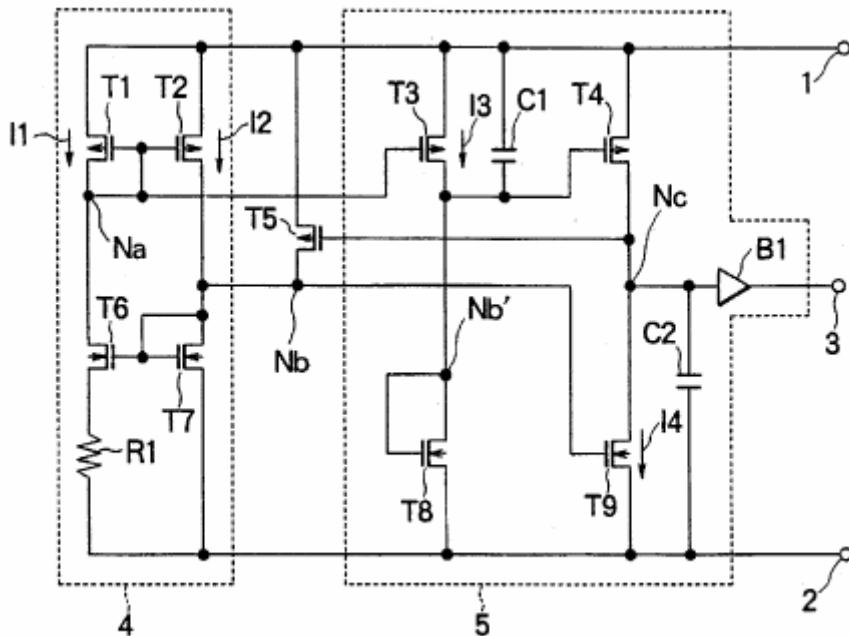


Figure 3 depicts a circuit that includes P-channel FETs **T1**, **T2**, **T3**, **T5**, and N-channel FETs **T6**, **T7**, **T8**, **T9**, resistor **R1**, capacitor **C2**, node **Nc** and output buffer **B1**.

The Examiner explains that Yokosawa describes that the potential **Vc** at the node **Nc** is determined in accordance with the values of the current driving capability **It4** of P-channel FET **T4** and the current driving capability of N-channel FET **T9**. (FF 7, Ans. 5-6). The Examiner determines that Yokosawa's description expressly states that the voltage at node **Nc** is the result of the comparison of currents **It4** and **I4** (Ans. 6).

The Applicant argues that an ordinarily skilled person would likely conclude that the current through Yokosawa's transistors **T4** and **T9** will be the same except for transient variations as capacitor **T2** (sic **C2**) charges and discharges (Reply Br. 2). In response, the Examiner concludes that the Applicant's statement would be true if one assumed that Yokosawa's buffer **B1** draws no current (Supplemental Ans. 2). The Examiner notes that the

Applicant has not proffered a description in Yokosawa that describes buffer **B1** as drawing no current (Supplemental Ans. 2). The Applicant has not presented sufficient evidence or persuasive arguments to support the contention that an ordinarily skilled person would likely conclude that the current through Yokosawa's transistors **T4** and **T9** will be the same. Argument of counsel cannot take the place of evidence lacking in the record. As a result, the Applicant has not shown that the Examiner erred.

The Applicant also argues that an ordinarily skilled person would conclude that the current-driving capability of transistors **T4** and **T9** reflects their physical structure, which can be different than the current that flows through the transistors, and therefore Yokosawa does not describe any element that compares the currents through **T4** and **T9** (Reply Br. 2-3).

The Examiner responded and explains that there is no distinction between the current-driving capability of a transistor and the current a transistor provides, since the current provided by a transistor is a direct function of its physical structure (i.e. channel size) and its operating state (Supplemental Ans. 3). The Examiner finds that Yokosawa's node **Nc** with capacitor **C2** indirectly compares the currents from the transistors **T4** and **T9** because those currents indirectly (by way of the voltage drops across the respective transistors) determine the voltage **Vc** at node **Nc** (Supplemental Ans. 4). The Examiner points out that buffer **B1** is a voltage responsive element and that the voltage drops across transistors **T4** and **T9** determine the voltage **Vc** at node **Nc** similar to Applicant's figure 2 arrangement where node **VN** and inverter **10** do not directly, but indirectly, compare the currents in transistors **7** and **9** (Supplemental Ans. 2-4). The Examiner concludes that utilizing the broadest reasonable interpretation of the claim language which is also

consistent with Applicant's disclosure, Yokosawa's circuit meets Applicant's claim language of "a current comparison circuit . . . comparing the first and second currents so as to provide a voltage at the output node based on the current comparison." (Supplemental Ans. 4).

The Applicant did not respond to the Examiner's Supplemental Answer.⁶ The rationale provided in the Examiner's Supplemental Answer is sound and persuasive. In support of the Examiner's explanation that current is a direct function of a transistor's driving capability, we note that Yokosawa interchanges the term "current driving capability" with the term "current" (FFs 8-10). As pointed out by the Examiner, Yokosawa describes that if **It4<I4**, the potential **Vc** at node **Nc** becomes a low level and if **It4>I4**, the potential **Vc** at node **Nc** becomes a high level (FF 11), which is similar to Applicant's output arrangement shown in Applicant's figure 2 (Supplemental Ans. 2-4). As a result, we disagree that the Examiner erred in finding that (1) Yokosawa's description of a transistor's driving capability is a direct function of the current flowing through the transistor, and (2) Yokosawa describes a comparison circuit (**Nc** and **C2**) that compares the currents through transistors **T4** and **T9** as claimed.

The Applicant's argument that an ordinarily skilled person would not regard Yokosawa's capacitor **C2** as the claimed current comparison circuit (Reply Br. 2) is also not persuasive and is misplaced. The Examiner found that *both* node **Nc** and capacitor **C2** are part of the current comparison circuit (FF 6) and that Yokosawa's node **Nc** in cooperation with capacitor **C2** indirectly compares the currents in the transistors **T4** and **T9** as already

⁶ If a supplemental examiner's answer is furnished by the examiner, appellant may file another reply brief ... Bd. R. 43(2)(b).

explained. The Applicant has not provided persuasive arguments or evidence to establish that capacitor **C2** does not form a part of a current comparison circuit. To reiterate, Yokosawa describes that if **It4<I4**, the potential **Vc** at node **Nc** becomes a low level and if **It4>I4**, the potential **Vc** at node **Nc** becomes a high level. Accordingly, the Yokosawa arrangement compares the first and second currents **It4** and **I4**, so as to provide a voltage at the output node based on the current comparison. Therefore, we are unable to find that the Examiner erred.

Lastly, the Applicant argues that Yokosawa's figure 3 is similar to the prior art arrangement described in Applicant's figure 1 and that the prior art arrangement has several drawbacks (Reply Br. 3). The Applicant attributes transistors **71** and **72** as corresponding to Yokosawa's transistors **T4** and **T9** and capacitor **73** as corresponding to Yokosawa's capacitor **C2**. The Examiner applied the broadest reasonable interpretation standard to Applicant's claims 5-7 and found that Yokosawa anticipates those claims. As stated above, the Applicant has not sufficiently demonstrated error in the Examiner's findings and rationale. The Applicant's argument that Yokosawa's figure 3 arrangement has common elements with the prior art arrangement described in Applicant's specification is of no consequence to the findings and extensive rationale provided by the Examiner.

For all these reasons we find that the Applicant has failed to sufficiently show that the Examiner erred in finding claims 5-7 are anticipated by Yokosawa under 35 U.S.C. § 102(b).

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Decision

Upon consideration of the record, and for the reasons given, the Examiner's rejection of claims 5-7 under 35 U.S.C. § 102(b) as anticipated by Yokosawa is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED

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