

The opinion in support of the decision being entered today was *not* written for publication and is *not* binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte BOHUMIL LOJEK and
PHILIP O. SMITH

Appeal 2007-1274
Application 10/850,897
Technology Center 2800

Decided: April 30, 2007

Before EDWARD C. KIMLIN, BRADLEY R. GARRIS, and CHUNG K. PAK, *Administrative Patent Judges*.

PAK, *Administrative Patent Judge*.

ORDER REMANDING TO THE EXAMINER
PURSUANT TO 37 C.F.R. § 41.50(a)

On this record, we determine that this case is not ripe for meaningful review and is, therefore, remanded to the Examiner for appropriate action not inconsistent with the instruction set forth below.

At pages 3 through 5 of the Answer, the Examiner set forth, *inter alia*, the following rejection:

1. Claims 7-13, 15[,] and 19-21 are rejected under 35 U.S.C. [§] 103(a) as being unpatentable over Rao et al. (US Pat. 6,808,986, hereinafter Rao) in view of Prall et al. (US Pat. 5,345,104, hereinafter Prall).

...

According to the Examiner (Answer 4):

Rao discloses in fig. 1 a memory device (col. 2, lines 13-58), comprising: a silicon substrate 12 having a layer of tunnel oxide 18 situated above a channel in the substrate 12; a floating gate (see Abstract) having silicon nanocrystals 20 therein disposed over the tunnel oxide layer 18; silicon nanocrystals 20 embedded in a control oxide layer 22; a polysilicon control gate 24 over the floating gate; and lateral nitride spacers 26 surrounding the floating gate stack.

Rao discloses a memory structures as describe[d] above but fails to disclose the spacers is [sic] formed of oxide layer. However, Prall teaches a similar memory structures having the oxide layer 22 as a spacers [sic] (col. 4, lines 13-20 and fig. 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Rao by forming the oxide spacers as taught by Prall since the material such as oxide/nitride layer is recognized equivalent material for forming the spacers in a memory device.

The Appellants argue (Br. 10) that:

[E]ven if such a modification would be obvious to one of skill in the art, it still would not result in Appellants' claimed invention because the oxide spacers taught by Prall et al. are significantly different from the thermal oxide spacers claimed by Appellants....

The Examiner asserts that the claimed “thermal oxide” spacer is no different from the prior art oxide spacer since the claimed “thermal oxide” spacer is an oxide spacer made from an oxide layer produced by thermal oxidation

(Answer 4-8 and Reply Br. 4). In other words, the claimed “thermal oxide” spacer is an oxide spacer further defined by a thermal oxidation process, which does not render the claimed spacer patentably distinct from the spacer suggested by the prior art references (*id.*).

To rebut the Examiner’s assertion, the Appellants rely on two evidence literatures, namely S.M. Sze, *VLSI Technology* 117-118 2d ed., McGraw-Hill, Inc. 1988) and S.K. Ghandhi, *VLSI Fabrication Principles* 529 (2d ed., John Wiley and Sons, Inc. 1994), extensively to demonstrate that the claimed thermally grown oxide spacer is patentably different from the oxide spacer made from a deposition process (Br. 11-13 and Reply Br. 5-6). However, it is not clear from the record whether the Examiner approved entry of the literature evidence relied upon by the Appellants. See the record in its entirety. Moreover, contrary to the Appellants’ arguments at pages 11 through 13 of the Brief, the “Evidence Appendix” at page 20 of the Brief states that the Appellants do not rely on any evidence.

We observe that the Examiner refers to the literature evidence relied upon by the Appellants at page 7 of the Answer. However, the Examiner does not indicate whether the literature evidence is entered into the record (*id.*). Nor does the Examiner address the sufficiency of the literature evidence relied upon by the Appellants (compare Answer 7-8 with Br. 11-13 and Reply Br. 5-6).

The Examiner also does not fully analyze the teachings of Rao. We note that Rao is not limited to forming a silicon nitride spacer as asserted by the Examiner. We note that Rao teaches that any dielectric layer can be used to form spacers (col. 2, ll. 46-48) and that the dielectric layer can include thermally grown or deposited silicon dioxide (col. 2, ll. 25-26).

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Therefore, pursuant to 37 C.F.R. § 41.50(a)(2004), we remand this application to the Examiner to:

- 1) Determine and notify the entry status of the literature evidence relied upon by the Appellants;
- 2) Notify the Appellants of the deficiencies or defectiveness of the Brief discussed above and provide an opportunity to submit a corrected Brief; and
- 3) Evaluate and address in the written record the sufficiency of the literature evidence, if entered, and the full teachings of Rao to determine the appropriateness of (i) maintaining the ground of rejection set forth in the Answer and (ii) making a new ground of rejection (and, if not, why not).

REMANDED/§ 41.50(a)

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Schneck & Schneck
P. O. Box 2-E
San Jose, CA 95109-0005