

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DEREK ORZO RICCI

Appeal 2007-1307
Application 10/454,274
Technology Center 2100

Decided: October 22, 2007

Before KENNETH W. HAIRSTON, JOHN C. MARTIN, and ROBERT E. NAPPI, *Administrative Patent Judges*.

HAIRSTON, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellant appeals under 35 U.S.C. § 134 from a final rejection of claims 1 to 12. We have jurisdiction under 35 U.S.C. § 6(b).

We reverse.

STATEMENT OF THE CASE

Appellant has invented a method that uses a data processing system for database bitmap index processing in a database management system. The data processing system uses a microprocessor with instructions for

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simultaneous processing of at least 128 bits and storage units of at least 128 bits for processing of bitmap index format database structures (Figure 1; Specification 2, 3, 8, 9, and 14).

Claim 1 is representative of the claims on appeal, and it reads as follows:

1. A computer-based method for database bitmap index processing in a database management system, the method comprising the steps of:

(a) utilizing a microprocessor supporting instructions for simultaneously processing of at least 128 bits and having storage units of at least 128 bits to process bitmap index format database structures.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Abrams	US 5,835,634	Nov. 10, 1998
Ginter	US 5,892,900	Apr. 6, 1999
Hathaway	US 5,978,898	Nov. 2, 1999
Bhashyam	US 6,618,729 B1	Sep. 9, 2003 (filed Apr. 20, 2000)

The Examiner rejected claims 1, 2, 5, 6, 9, and 10 under 35 U.S.C. § 103(a) based upon the teachings of Bhashyam and Hathaway. The Examiner rejected claims 3, 7, and 11 under 35 U.S.C. § 103(a) based upon the teachings of Bhashyam, Hathaway, and Ginter. The Examiner rejected claims 4, 8, and 12 under 35 U.S.C. § 103(a) based upon the teachings of Bhashyam, Hathaway, and Abrams.

Appellant contends *inter alia* that the applied references, whether considered separately or in combination, do not teach or suggest “utilizing a microprocessor supporting instructions for simultaneous processing of at

least 128 bits and having storage units of at least 128 bits to process bitmap index format database structures” as set forth in claims 1, 5, and 9 on appeal (Reply Br. 13, 14, 25, 30, and 31).

ISSUE

Does the applied prior art teach or would it have suggested to the skilled artisan all of the features of the claimed invention?

FINDINGS OF FACT

1. Appellant describes “a method and system for highly efficient database bitmap index processing” (Specification 1).
2. Appellant states “modern relational database management systems include the capability to use bitmap indexes as an index format” (Specification 2).
3. The described method “utilizes a microprocessor supporting instructions for simultaneous processing of at least 128 bits and having storage units of at least 128 bits to process bitmap index format database structures” (Specification 3).
4. Appellant states that:

On common processors, such as Intel Pentium, these storage units can be 8-bit (byte), 16-bit (word), or 32-bit (double word). In a 32-bit processor (like the Intel Pentium), it is more efficient to process bitmaps in 32-bit storage units, rather than in 8-bit storage units, because the internal parallelism inherent in a 32-bit processor allows fewer instructions, memory accesses, and loop iterations needed to process a bitmap of given size. For example, given a 4000 byte bitmap, Intel Pentium could process an AND instruction 4000 times on 8-bit storage units, or could process the AND instruction 1000 times on 32-bit storage units. Since it takes approximately the same amount of time for each individual AND

instruction, regardless of whether it processes an 8-bit or 32-bit storage unit, it is significantly faster to process the larger bitmap storage units, such as 32-bit storage units. However, processing bitmaps, even in 32-bit storage units, uses significant computer processor and memory resources.

Moreover, this problem increases as the number and size of bitmaps increases.

(Specification 8).

5. Appellant indicates that “processing the bitmaps in 128-bit storage units, rather than in 32-bit storage units, significantly improves efficiency and speed by reducing the number of instructions, memory accesses, and loop iterations needed to process a bitmap of given size” (Specification 9).

6. Bhashyam was cited by the Examiner merely because it “relates in general to database management systems performed by computers, and in particular, to the optimization of a star join operation in a relational database management system using a bitmap index structure” (col. 1, ll. 9 to 12)¹ (Answer 4).

7. Hathaway was cited by the Examiner because he “teaches allocating registers in a superscalar machine (See abstract), in which he teaches utilizing a microprocessor supporting instructions for simultaneous processing of at least 128 bits and having storage units of at least 128 bits to process bitmap index format database structures (See column 1, lines 10-14, lines 54-59, where ‘register’ is read on ‘storage units’)” (Answer 4).

8. Ginter was cited by the Examiner for a teaching of “systems and methods for secure transaction management and electronic rights protection (See

¹ Compare the referenced teaching in Bhashyam with the acknowledged prior art teaching in Appellant’s disclosure described *supra* in finding of fact number 2.

abstract), in which he teaches wherein the instructions being assembly language instructions (See column 231, lines 46-51); a second instruction for performing a logical AND instruction on the two storage units of at least 128 bits (See column 76, lines 51-59)” (Answer 8).

9. Abrams was cited by the Examiner for a teaching of “bitmap comparison apparatus and method sing [sic, using] an outline mask and differently weighted bits (See abstract), in which he teaches wherein a join operation on two bitmap indexes being performed by comparing two bitmap indexes and computing their intersection using a logical AND instruction (See abstract; column 4, lines 43-44; column 9, lines 19-29; column 10, lines 31-32)” (Answer 9).

PRINCIPLES OF LAW

The Examiner bears the initial burden of presenting a *prima facie* case of obviousness. *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). The Examiner’s articulated reasoning in the rejection must possess a rational underpinning to support the legal conclusion of obviousness. *In re Kahn*, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006).

“One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention.” *In re Fine*, 837 F.2d 1071, 1075, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988).

In an obviousness rejection, it is impermissible “to pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art.” *In re Wesslau*, 353 F.2d 238, 241, 147 USPQ 391, 393 (CCPA 1965).

ANALYSIS

It is abundantly clear from the findings of fact that the applied references neither teach nor would have suggested to one of ordinary skill in the art “utilizing a microprocessor supporting instructions for simultaneous processing of at least 128 bits and having storage units of at least 128 bits to process bitmap index format database structures” as set forth in the claims on appeal. As indicated *supra* in findings of fact numbers 2 and 6, the teachings of Bhashyam mirror the prior art acknowledgment in Appellant’s disclosure. The 128-bit register status bit vector described in Hathaway is not relevant to the 128 bits processed during the processing of “bitmap index format database structures” in the claims on appeal. Accordingly, we agree with the Appellant’s arguments throughout the Briefs that the claimed invention is neither taught by nor would have been suggested by the applied references.

The teachings of the references to Ginter and Abrams fail to cure the noted shortcoming in the teachings of Bhashyam and Hathaway.

CONCLUSION OF LAW

In the obviousness rejection, the Examiner used impermissible hindsight reconstruction to pick and choose among disclosures in the applied prior art references. Obviousness has not been established by the Examiner because the applied references neither teach nor would have suggested to the skilled artisan the claimed invention.

ORDER

The obviousness rejection of claims 1 to 12 is reversed.

OTHER ISSUES

In view of Appellant's disclosure of presumably commonly known teachings described *supra* in connection with findings of fact numbers 2, 4, and 5, and recent case law concerned with obviousness, the Examiner should consider instituting a new obviousness rejection of at least claims 1, 5, and 9 if, in fact, it was well known to artisans to use either 8-bit registers, 16-bit registers, and 32-bit registers in connection with database bitmap index format processing. If the processing speed increases with the size of the register, then it is expected that a 128-bit register will process the bits at an even greater speed than the 8-bit register, the 16-bit register or the 32-bit register. "If a person of ordinary skill can implement a predictable variation, § 103 likely bars its patentability." *KSR Int'l v. Teleflex, Inc.*, 127 S. Ct. 1727, 1740, 82 USPQ2d 1385, 1396 (2007). If 8-bit, 16-bit, and 32-bit registers were indeed known and used by the skilled artisan for bitmap index processing, then it follows that it would have been "obvious to try" even larger bit-size registers for bitmap index processing. *KSR*, 127 S. Ct. at 1742, 82 USPQ2d at 1397.

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