The opinion in support of the decision being entered today was *not* written for publication and is *not* binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KIRAN V. CHATTY, PETER E. COTTRELL,
ROBERT J. GAUTHIER, JR., and MUJAHID MUHAMMAD

Appeal 2007-1360
Application 10/605,699
Technology Center 2800

Decided: June 26, 2007

Before JOHN C. MARTIN, JOSEPH F. RUGGIERO, and ALLEN R. MACDONALD, *Administrative Patent Judges*.

RUGGIERO, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134 from the Final Rejection of claims 1-31. We have jurisdiction under 35 U.S.C. § 6(b).

Appellants' claimed invention relates to a system and method for suppressing latch-up within integrated circuits. Based on a recognition that

the farther a latch-up structure is from the current injection point the fewer the carriers that will be available for structure latch-up, the invention provides for greater contact periodicity in areas of the integrated circuit remote from the injection source. (Specification, paragraphs [0021] and [0041].

We affirm.

Claim 1 is illustrative of the invention and it reads as follows:

1. A CMOS semiconductor substrate comprising:

a substrate;

a plurality of circuit structures formed upon said substrate, wherein at least one of said circuit structures has a susceptibility to a latch-up condition;

an injection site associated with said CMOS semiconductor structure; and

a plurality of contact regions inter-spaced a varying distance between said circuit structures.

The Examiner relies on the following prior art references to show unpatentability:

Magee	US 4,642,667	Feb. 10, 1987
Kim	US 5,675,170	Oct. 7, 1997

Claims 1-10 and 15-31 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Kim. Claims 1, 7, and 11-14 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Magee.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the Briefs and Answer for the respective details. Only

those arguments actually made by Appellants have been considered in this decision. Arguments which Appellants could have made but chose not to make in the Briefs have not been considered and are deemed waived [see 37 C.F.R. § 41.37(c)(1)(vii)].

ISSUES

(i) Under 35 U.S.C § 102(b), does Kim have a disclosure which anticipates the invention set forth in claims 1-10 and 15-31?

(ii) Under 35 U.S.C § 102(b), does Magee have a disclosure which anticipates the invention set forth in claims 1, 7, and 11-14.

PRINCIPLES OF LAW

It is axiomatic that anticipation of a claim under § 102 can be found if the prior art reference discloses every element of the claim. *See In re King*, 801 F.2d 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1986) and *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1458, 221 USPQ 481, 485 (Fed. Cir. 1984).

In rejecting claims under 35 U.S.C. § 102, a single prior art reference that discloses, either expressly or inherently, each limitation of a claim invalidates that claim by anticipation. *Perricone v. Medicis Pharm. Corp.*, 432 F.3d 1368, 1375-76, 77 USPQ2d 1321, 1325-26 (Fed. Cir. 2005), citing *Minn. Mining & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc.*, 976 F.2d 1559, 1565, 24 USPQ2d 1321, 1326 (Fed. Cir. 1992). Anticipation of a patent claim requires a finding that the claim at issue "reads on" a prior art reference. *Atlas Powder Co. v. IRECO, Inc.*, 190 F.3d 1342, 1346, 51 USPQ2d 1943, 1945 (Fed. Cir. 1999) ("In other words, if granting patent

protection on the disputed claim would allow the patentee to exclude the public from practicing the prior art, then that claim is anticipated, regardless of whether it also covers subject matter not in the prior art.") (internal citations omitted).

ANALYSIS

With respect to the 35 U.S.C. § 102(b) rejection of independent claims 1 and 22 based on the teachings of Kim, the Examiner indicates (Answer 3) how the various limitations are read on the disclosure of Kim. In particular, the Examiner directs attention to the illustrations in Figures 3 and 4 of Kim, as well as the disclosure at column 3, lines 8-16 of Kim.

Appellants' arguments in response assert that the Examiner has not shown how each of the claimed features is present in the disclosure of Kim so as to establish a prima facie case of anticipation. Appellants' arguments (Br. 7-8) focus on the contention that, in contrast to the requirements of independent claims 1 and 22, Kim does not disclose an injection site associated with a CMOS semiconductor structure.

As pointed out by the Examiner, however, Kim discloses (col. 2, ll. 34-42) the structural interconnection of the injection site (data I/O pad) and the PMOS and NMOS transistors which make up the CMOS semiconductor structure. With this explicit disclosure of Kim in mind, we fail to see how Kim's data I/O pad injection site could be considered to be anything other than "associated" with the CMOS semiconductor structure as claimed.

Appellants have further expanded (Reply Br. 2-4) upon this argument by attempting to draw a distinction between Kim's injector site which, according to Appellants, is located on the surface of the semiconductor

device and Appellants' injector site which, Appellants argue, is located "within the semiconductor structure." It is apparent to us, however, that, to whatever extent Appellants are relying on a particular physical location of the claimed injector site relative to the overall CMOS semiconductor device to distinguish over Kim, no such physical location is specified in the claims. It is our opinion that Appellants' arguments improperly attempt to narrow the scope of the claim by implicitly adding disclosed limitations which have no basis in the claim. *See In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997).

We are further of the view, after reviewing Appellants' Specification, that there is simply no support in Appellants' disclosure for the interpretation of the claim language "injection site associated with said CMOS semiconductor structure" urged by Appellants in the Briefs. For example, paragraph [0042], lines 8-11 of Appellants' Specification states "[t]hus, an injector represents any possible source, or combination of sources, of current to the IC, either internal current injector (on-chip injector) or external current injector (off-chip injector)."

Further, as with Appellants' earlier arguments, we find Appellants' contention (Br. 8; Reply Br. 4) that Kim's latch-up prevention guard ring structure, which is placed under the data I/O pad, is not applicable to modern CMOS technologies to be not commensurate with the scope of the claims. We find no language of any kind in independent claims 1 and 22 which precludes the use of latch-up preventing guard rings as disclosed by Kim.

In view of the above discussion, since all of the claimed limitations are present in the disclosure of Kim, the Examiner's 35 U.S.C. § 102(b) rejection, based on Kim, of independent claims 1 and 22, as well as

dependent claims 2-4, 7-10, 15-18, 20, 21, 23-25, 28, 30, and 31 not separately argued by Appellants, is sustained.

We also sustain the Examiner's 35 U.S.C. § 102(b) rejection, based on Kim, of dependent claims 19 and 29 which set forth the use of the claimed latch-up prevention CMOS semiconductor structure to prevent latch-up from a cable discharge. We find no error in the Examiner's position (Answer 5, 8) that such claim language is a mere recitation of intended use and does not serve to distinguish over the CMOS semiconductor structure disclosed by Kim. Further, the record before us is totally devoid of any evidence to support Appellants' contention (Br. 8) that Kim's disclosed structure would not be applicable to what Appellants have termed "non-standard" latch-up tests "arising from a cable discharge event" due to Kim's requirement for a large N-well guard ring for latch-up prevention.

Turning to a consideration of the Examiner's 35 U.S.C. § 102(b) rejection of dependent claims 5, 6, 26, and 27, based on Kim, we sustain this rejection as well. Appellants argue (Reply Br. 5) that Kim does not disclose the spacing of contact regions 22, 23, and 41 which "*varies with the proximity*" of the contact regions to the injection site. We do not find this persuasive since the language quoted by Appellants appears only in dependent claims 2 and 23. On the other hand, dependent claims 5, 6 and 26, 27 are ultimately dependent, respectively, on claims 4 and 25, which depend, respectively, from independent claims 1 and 22 and do not include claims 2 and 23 in their dependency chain.

We also sustain the Examiner's 35 U.S.C. § 102(b) rejection of claims 1, 7, and 11-14 based on Magee. Appellants' arguments in response (Br. 9-10; Reply Br. 5-7) mirror those made with respect to Kim, and we find such

arguments to be equally unpersuasive. We agree with the Examiner's finding (Answer 5-6) that Magee discloses a latch-up susceptible CMOS semiconductor structure (col. 1, l. 62 through col. 3, l. 53) associated with an I/O injector site and having plural contact regions 32-36 which are spaced a varying distance between the circuit structures. As such, it is apparent to us that Magee discloses all that is claimed in appealed claims 1, 7, and 11-14. We would also point out that Appellants' argument (Br. 10) that Magee "teaches away" from the claimed invention is not appropriate or persuasive in a rejection based on anticipation.

CONCLUSION

In summary, we have sustained the Examiner's rejections of all the claims on appeal. Therefore, the decision of the Examiner rejecting claims 1-31 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

KIS

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