UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte RODNEY W. SCHMIDT, BRIAN C. BARNES,
GEOFFREY S. STRONGIN, and DAVID S. CHRISTIE

Appeal 2007-1501
Application 10/161,500[1]
Technology Center 2100

Decided: December 21, 2007

Before JAMES D. THOMAS, JAY P. LUCAS, and SCOTT R. BOALICK, *Administrative Patent Judges*.

LUCAS, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF CASE

Appellants appeal from a final rejection of claims 1 to 57[2] under authority of 35 U.S.C. § 134. The Board of Patent Appeals and Interferences (BPAI) has jurisdiction under 35 U.S.C. § 6(b).

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[1] Application filed May 31, 2002. The real party in interest is Advanced Micro Devices, Inc.

Appellants' invention relates to solid state computer devices. When these microcomputers malfunction, creating an error condition (which they call an "exception"), certain key information is stored in a table in memory called the exception stack frame. This information, including the last instruction to be executed and various pointers, is useful in determining what caused the error condition. In the words of the Appellants:

> According to one aspect of the present invention, a method is provided. The method includes creating a security exception stack frame in secure memory at a base address. The method also includes writing a faulting code sequence address and one or more register values into the security exception stack frame, and executing a plurality of security exception instructions.
>
> (Spec. 4-5.)

Claim 1 is exemplary:

> 1. A method, comprising:
>
> creating a security exception stack frame within secure memory at a base address;
>
> writing a faulting code sequence address and one or more register values into the security exception stack frame; and

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[2] Claims 23 to 35 have been indicated as being allowable. (Examiner's Answer, 23). They have not been argued by the Examiner or the Appellants. However, the Examiner has also indicated in the Answer, page 2, that they were also part of the subject of the Appeal. We treat them in this Opinion as being allowed.

executing a plurality of security exception instructions.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Wise	US 6,330,666 B1	Dec. 11, 2001
Andress	US 6,697,959 B2	Feb. 24, 2004 (filed Dec. 20, 2000)
Eldredge	US 6,792,499 B1	Sep. 14, 2004 (filed Feb. 1, 2002)
Ellison	US 6,957,332 B1	Oct. 18, 2005 (filed Mar. 31, 2000)

Rejections:

R1: Claims 1, 2, 6, 7, 8, 9, 10, 16, 17, 18, 19, 21, 36, 40, 44, 48, 49, 53, and 56 are rejected under 35 U.S.C. § 102(e) as being anticipated by Andress.

R2: Claims 3, 4, 5, 13, 22, 37, 38, 39, 41, 45, 46, 47, and 57[3] are rejected under 35 U.S.C. § 103(a) as being unpatentable over Andress in view of Ellison.

R3: Claims 11, 12, 20, 50, and 51 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Andress in view of Eldredge.

[3] See Other Issues for a comment on the dependency of claim 57.

R4: Claims 14, 15, 42, 43, 54, and 55 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Andress in view of Wise.

R5: Claim 52 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Andress in view of Eldredge and further in view of Ellison.

Appellants contend that the claimed subject matter is not anticipated by Andress, or rendered obvious by Andress in combination with Ellison, Eldredge, or Wise for reasons to be discussed more fully below. The Examiner contends that each of the five groups of claims is properly rejected.

Rather than repeat the arguments of Appellants or the Examiner, we make reference to the Briefs and the Answer for their respective details. Only those arguments actually made by Appellants have been considered in this decision. Arguments which Appellants could have made but chose not to make in the Briefs have not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii) (2004).[4]

We affirm the rejections.

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[4] Appellants have not presented any substantive arguments directed separately to the patentability of the dependent claims or related claims in each group, except as will be noted in this opinion. In the absence of a separate argument with respect to those claims, they stand or fall with the representative independent claim. *See In re Young,* 927 F.2d 588, 590 (Fed. Cir. 1991).

ISSUE

The issue is whether Appellants have shown that the Examiner erred in rejecting the claims under 35 U.S.C. § 103(a). The issue turns on whether Andress teaches that a security exception stack frame is known to be created within a secure memory at a base address, as claimed.

Appellants and the Examiner have developed the issue to depend on a single finding concerning the teaching of the stack in a secure memory in Andress. All rejections under 35 U.S.C. § 102 or § 103 have been argued using the same contention. (App. Br. 10, bottom; 11, middle; 12, middle; 13, bottom; 14, bottom).

FINDINGS OF FACT

The record supports the following findings of fact (FF) by a preponderance of the evidence.

1. Appellants claim a method, system and program (hereinafter method) for creating a security exception stack frame within secure memory at a base address. Secure memory is not formally defined in the Specification, but the placement is set at boot time (Spec. 22, l. 7) and includes security bits and other security measures to protect the data in the stack frame from being overwritten. (Spec. 24, l. 24).

2. Andress teaches a data processing device and method with special fault handling subsystems. Andress improves on the prior art (Col. 8, l. 25) in

a number of ways, but relevant to Appellants' claims it protects memory areas from inadvertently being overwritten. (Col. 8, l. 43). In that protected area is stored a save store stack frame. See (Col. 9, l. 4) (Col. 9, l. 35), among other structures. The protected area is described as being a reserve area 85, which cannot be inadvertently written. See the description in Column 9, line 50+, and Column 6, line 10.

PRINCIPLES OF LAW

Appellants have the burden on appeal to the Board to demonstrate error in the Examiner's position. See *In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006) ("On appeal to the Board, an applicant can overcome a rejection [under § 103] by showing insufficient evidence of prima facie obviousness or by rebutting the prima facie case with evidence of secondary indicia of nonobviousness.") (quoting *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998)).

"In reviewing the [E]xaminer's decision on appeal, the Board must necessarily weigh all of the evidence and argument." *In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992).

It is axiomatic that anticipation of a claim under § 102 can be found only if the prior art reference discloses every element of the claim. See *In re King*, 801 F.2d 1324, 1326 (Fed. Cir. 1986) and *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1458 (Fed. Cir. 1984).

ANALYSIS

From our review of the administrative record, we find that Examiner has presented prima facie cases for the rejections of Appellants' claims under 35 U.S.C. §§ 102 and 103. The prima facie cases are presented on pages 3 to 10 of the Examiner's Answer.

Rejection under 35 U.S.C. § 102(e)

In opposition, Appellants present one main argument. Appellants contend that

> the safe store buffer 286 is not a secure memory. To the contrary, the safe store buffer 286 is just a buffer in a central processing unit 92…. Thus, Andress fails to teach or suggest writing a faulting code sequence address into a security exception stack frame within a <u>secure memory</u>, as set forth in independent claims 1, 16, 23, 36, 44 and 56.
>
> (App. Br. 10.)

We reviewed the Andress reference, and found that it presents a structure to overcome faults in operation of the microprocessor. To maintain evidence of the data environment during a system fault, two safe store stack frames are created. (Col. 8, ll. 19, 24).

Andress exhibits an explicit appreciation of the problem of overwriting memory areas during malfunctions. (Col. 8, l. 41+). As such, the reference teaches that all "fault handlers, as well as the descriptors to it, are stored in reserved memory 85" to prevent their being overwritten. In

every aspect the nature of the reserved memory 85 can be read on the claimed limitation "secure memory." "Reserved memory cannot be written inadvertently. It is never made part of any work space, nor ever framed by a segment descriptor 302." (Col. 9, l. 50). We therefore find that the reference teaches protecting safe store (security exception) stack frames in the protected reserve memory, as claimed.

In the Reply Brief, Appellants argue that since the reserved memory 85 may be used regardless of any security features, it is not associated with the security of the computer system. (Reply Br. 2, middle). We read Andress to indicate that the reserved memory is independent of whatever type of security features are used, and not to indicate that it obviates security measures at all, or is disassociated with them.

We thus do not find error in the Examiner's rejection of claims 1, 2, 6 to 10, 16 to 19, 21, 36, 40, 44, 48, 49, 53, and 56 under Andress.

Rejection under 35 U.S.C. § 103(a)

Appellants have argued rejections R2 to R5 using the same reasoning stated above, concerning Andress not teaching secure memory. As we have found that Andress does provide such a teaching with respect to his reserved memory, and that there are no other independent issues before us, we thus find no error in the four rejections under 35 U.S.C. § 103(a).

CONCLUSION OF LAW

Based on the findings of facts and analysis above, we conclude that the Examiner did not err in rejecting claims 1 to 22 and 36 to 57.

DECISION

The Examiner's rejection of claims 1 to 22 and 36 to 57 is affirmed.

OTHER ISSUES

Examiner noted that claim 31, a system claim, is improperly dependent on claim 13, a method claim. He assumed that claims 31 and 32 were intended to be dependent on allowable claim 23, and we followed that assumption. (Ans. 2.) Similarly, claim 57, a method claim, is improperly dependent on claim 56, a system claim. We have assumed that this was a typographical error, and claim 57 was intended to be a system claim dependent on claim 56.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED

rwk

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