

The opinion in support of the decision being entered today is *not* binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte TODD A. RANDAZZO, BRIAN E. BURDICK,
and EDSON W. PORTER

Appeal 2007-1540
Application 10/280,788
Technology Center 2100

Decided: July 25, 2007

Before FRED E. McKELVEY, *Senior Administrative Patent Judge*,
ALLEN R. MacDONALD, and ROBERT E. NAPPI, *Administrative Patent Judges*.

NAPPI, *Administrative Patent Judge*.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 6(b) of the Final Rejection of claims 17, 18, 20, and 21. For the reasons stated *infra*, we affirm the Examiner's rejection of these claims.

INVENTION

The invention is directed to an input buffer which protects an integrated circuit from overvoltage conditions. See page 2 of Appellants' Specification. Claim 17 is representative of the invention and reproduced below:

17. A high speed input buffer electrically connected to an input voltage pad, the high speed input buffer comprising:

a native transistor having a first contact electrically connected to the input voltage pad,

a single ended input circuit electrically connected to a second contact of the native transistor, and

a leakage element having a first electrical connection and a second electrical connection, the first electrical connection of the leakage element directly connected to the second contact of the first native transistor and the second electrical connection of the leakage element electrically connected to a VSS line, where the leakage element is one of a single NMOS transistor where a gate contact of the NMOS transistor is electrically connected only to the second contact of the native transistor, and a resistor.

REFERENCES

The references relied upon by the Examiner are:

Nakakura	US 5,512,844	Apr. 30, 1996
Metzler	US 6,420,757 B1	Jul. 16, 2002
Cress	US 6,483,386 B1	Nov. 19, 2002

REJECTIONS

Claims 17, 18, and 20 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Nakakura in view of Cress.

Claim 21 stands rejected under 35 U.S.C. § 103(a) as unpatentable over Nakakura in view of Cress and Metzler.

Appellants contend that the Examiner's rejections under 35 U.S.C. § 103(a) are in error. Appellants assert that Nakakura does not teach using a native transistor and that while Cress teaches a native transistor, the clamp circuit of Cress comprises two transistors rather than a leakage circuit with a resistor or single transistor as claimed. Brief, p. 4.

We are not persuaded by Appellants' arguments. Each of independent claims 17, 20, and 21 recites a circuit with a native transistor connected to an input pad and a single end input circuit. Each of the independent claims also recites a leakage element "directly connected to the second contact of the first native transistor and the second electrical connection of the leakage element electrically connected to a VSS line," where the leakage element is "a single NMOS transistor where a gate contact of the NMOS transistor is electrically connected only to the second contact of the native transistor."¹

Cress teaches a circuit using a native transistor to provide high voltage protection for a single ended input circuit. Abstract and col. 2, ll. 47-52. The native transistor provides protection when a low voltage circuit is connected to another circuit that operates at a higher voltage. Col. 1, ll. 15-19. The native transistor M3 is connected between an input signal line and

¹ Claims 17 and 20 recite that the leakage element alternatively is a resistor.

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the input of an amplifier. Col. 2, ll. 44-47. The gate of the native transistor M3 is supplied with a regulated signal, $Lv_{13}COMP_{13}EN$, such that the voltage output of the transistor will not be higher than the regulated supply VCC. Col. 2, ll. 58-62. The native transistor has a very low threshold voltage, which eliminates the dead zone and allows for input protection because of the regulated signal applied to the gate. Col. 3, ll. 18-29. A clamp circuit, item **104**, is connected between the output of the native transistor and the input of the amplifier. Col. 2, ll. 44-47. The clamp circuit contains two transistors M1 and M2, transistor M1 is configured to act as a diode. Col. 2, ll. 66-67 and Col. 3, ll. 44-50. Cress describes the input signal to transistor M2 as an enable to control the clamp, i.e. M2 functions as a switch to either electrically connect or disconnect transistor M1 to the circuit. Col. 3, ll. 29-32.

One skilled in the art would recognize that the functional equivalent of a closed switch is hard wiring the circuit, i.e. placing a direct connection in place of the switch. On the issue of obviousness the Supreme Court has recently stated that “when a patent claims a structure already known in the prior art that is altered by the mere substitution of one element for another known in the field, the combination must do more than yield a predictable result.” *KSR Int’l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1740, 82 USPQ2d 1385, 1395 (2007). In this case, we find that the substitution of a direct connection for the switch of transistor M2 to be a substitution of known elements, which will provide the predictable result of keeping the diode transistor M3 enabled, i.e. keeping the circuit in one of its known states. As such, we conclude the arrangement of Cress’s circuit with the diode

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connected transistor M1 directly connected to a contact of the native device would have been obvious. Accordingly, we affirm the Examiner's rejection of claims 17, 18, 20, and 21 under 35 U.S.C. § 103(a). However, as our decision relies upon different rationale than applied by the Examiner, we designate it a new rejection.

37 C.F.R. § 41.50(b) provides that the Appellants, WITHIN TWO MONTHS FROM THE DATE OF THE DECISION, must exercise one of the following two options with respect to the new ground of rejection to avoid termination of the appeal as to the rejected claims:

(1) *Reopen prosecution.* Submit an appropriate amendment of the claims so rejected or new evidence relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the proceeding will be remanded to the examiner. . . .

(2) *Request rehearing.* Request that the proceeding be reheard under § 41.52 by the Board upon the same record. . . .

AFFIRMED
37 C.F.R. § 41.50(b)

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