

The opinion in support of the decision being entered today is
not binding precedent of the Board

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JOHN ALAN WICKERAAD

Appeal 2007-1957
Application 09/561,179
Technology Center 2100

Decided: August 7, 2007

Before KENNETH W. HAIRSTON, JOSEPH F. RUGGIERO, and
MAHSHID D. SAADAT, *Administrative Patent Judges*.

SAADAT, *Administrative Patent Judge*.

STATEMENT OF THE CASE

Appellant appeals under 35 U.S.C. § 134(a) from the Examiner's Final Rejection of claims 1 and 3-25, which are all of the claims pending in this application as claim 2 has been canceled. We have jurisdiction under 35 U.S.C. § 6(b).

Appellant's invention relates to error logging and changing error levels from any level to other levels (Specification 2). According to Appellant, instead of classifying the errors in predetermined levels of

severity, the associated error level may be selected from a plurality of error levels to redefine the error level (*id.*).

Independent claims 1 and 10 read as follows:

1. A method using registers within a processor for indicating errors in a data processing system with a plurality of error levels, comprising steps of:

indicating that an error corresponds to one error level of said plurality of error levels;

representing said error with a set of memory cells;

defining said error in at least one of a plurality of error enable registers, wherein each of said plurality of error enable registers corresponds to one of said plurality of error levels; and

changing the error level of said error to another error level of said plurality of error levels, such that errors logged from power on will not cause said data processing system to go to a fatal error level so fast that it becomes difficult to debug said data processing system when said data processing system is powered on.

10. A data processing system, having an associated error level chosen from a plurality of error levels for an error, comprising:

a set of memory cells, including

a primary error log to record said error, and

at least one error enable register that can be read and written to redefine the error level of said error to one of said plurality of error levels.

The prior art references relied upon by the Examiner in rejecting the claims on appeal are:

Yamaguchi
Gervais

US 5,155,731
US 5,448,725

Oct. 13, 1992
Sep. 5, 1995

Myers	US 5,787,095	Jul. 28, 1998
Quach	US 6,636,991 B1	Oct. 21, 2003
		(filed Dec. 23, 1999)

Hennessy, "Computer Organization and Design; The Hardware/Software Interface," Morgan Kaufmann Publishers, Inc., 1998, pp. 225, 227, 229, 230.

Claims 10-13, 15-20, 22, and 23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Quach and Hennessy.

Claims 1, 3, 4, and 6-9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Quach, Hennessy, and Myers.

Claims 14, 21, and 25 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Quach, Hennessy, and Yamaguchi.

Claim 24 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Quach, Hennessy, and Gervais.

Claim 5 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Quach, Hennessy, Myers, and Yamaguchi.

We reverse.

ISSUE

The issue is whether Appellant has shown that the Examiner erred in rejecting the claims under 35 U.S.C. § 103. The issue turns on whether there is a legally sufficient justification for combining the disclosures of Quach and Hennessy and if so, whether the combination teaches the claimed subject matter. Specifically, the issue is:

whether a person of ordinary skill in the art would have added the field arrangement of bits in a word of Hennessy to the error signaling mechanism disclosed in Quach to arrive at the claimed subject matter.

FINDINGS OF FACT

The following findings of fact (FF) are believed to be supported by a preponderance of the evidence and relevant to the issue at hand.

1. Quach describes a processor error handling logic for controlling the way a processor generates signaling mechanism for specific types of error by promoting or demoting the signaling mechanism of specific error types (col. 2, ll. 40-45).

2. Quach further discloses that a signaling mechanism is associated with each soft error type that allows prioritization or treating the various error types with different levels of urgency (col. 3, ll. 57-61).

3. As shown in Figure 3, a method for promoting/demoting a signaling mechanism starts with programming the machine specific register 150 and includes the step of classifying the detected error (col. 5, ll. 14-25) and assigning the error to a signaling mechanism (col. 5, ll. 29-41).

4. Hennessy relates to computer organization and describes that bit fields or fields may be defined within words in C operation (p. 227).

5. Myers discloses a computer system with a second redundant signal line which includes error checking circuitry for indicating error if the signal on the two bus lines differ (Abstract).

6. Myers describes that fatal errors are signaled when hardware detects use of corrupt data which compromises data integrity (col. 20, ll. 14-

20) which requires a response such as stopping the computer and restarting in order to prevent corrupt data from entering the system (col. 20, ll. 32-36).

PRINCIPLES OF LAW

A claimed invention is unpatentable as obvious “if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” *See* 35 U.S.C. § 103(a) (2002); *In re Dembicza*k, 175 F.3d 994, 998, 50 USPQ2d 1614, 1616 (Fed. Cir. 1999).

“The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results.” *Leapfrog Enter., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157, 1161, 82 USPQ2d 1687, 1691 (Fed. Cir. 2007) (quoting *KSR Int'l v. Teleflex, Inc.*, 127 S. Ct. 1727, 1739-40, 82 USPQ2d 1385, 1395 (2007)). “One of the ways in which a patent's subject matter can be proved obvious is by noting that there existed at the time of invention a known problem for which there was an obvious solution encompassed by the patent's claims.” *KSR*, 127 S. Ct. at 1742, 82 USPQ2d at 1397. Design incentives and market forces as well as implementing a predictable variation may also help the person of ordinary skill in the art to recognize the obviousness of claimed combinations of elements of prior art. *KSR*, 127 S. Ct. at 1740, 82 USPQ2d at 1396.

Alternatively, a holding of obviousness can be based on a showing that there was “an apparent reason to combine the known elements in the fashion claimed.” *KSR*, 127 S. Ct. at 1740-41, 82 USPQ2d at 1396. In other words, “there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *Id.*, 127 S. Ct. at 1741, 82 USPQ2d at 1396 (quoting *In re Kahn*, 441 F.3d 977, 987, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006)). However, this reasoning is not limited to the problem the patentee was trying to solve; “any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed,” *KSR*, 127 S. Ct. at 1742, 82 USPQ2d at 1397 (emphasis added).

Furthermore, a reference may be understood by the artisan as suggesting a solution to a problem that the reference does not discuss. *See KSR*, 137 S. Ct. at 1742, 82 USPQ2d at 1397 (“Common sense teaches . . . that familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle. . . . A person of ordinary skill is also a person of ordinary creativity, not an automaton.”).

Further, a rejection based on section 103 must rest upon a factual basis rather than conjecture, or speculation. “Where the legal conclusion [of obviousness] is not supported by the facts it cannot stand.” *In re Warner*, 379 F.2d 1011, 1017, 154 USPQ 173, 178 (CCPA 1967). *See also In re Lee*, 277 F.3d 1338, 1344, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002) and *In re Kahn*, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006).

ANALYSIS

With respect to the teachings of Quach, we agree with Appellant's argument (Br. 17) that the demotion and promotion described in Quach relates to the signaling mechanism of specific error types (FF 1-3) which defines how the processor treats the errors. The Examiner has not identified any teachings in Quach related to changing and redefining the error level within the error log.

The Examiner further relies on Hennessy for a set of memory cells in the form of a plurality of registers (Answer 12-13) but fails to explain how the general description of fields and bits arrangement in a register cures the deficiency of Quach, as discussed above. Although the use of registers for storing errors is mentioned in Quach (FF 3) and Hennessy describes using registers in general (FF 4), nothing in these references discloses an error enable register that can be read and written to redefine the error levels.

The rationale argued by the Examiner for combining Quach and Hennessy is based on Hennessy disclosing "C allows bit fields or fields to be defined within words ... All fields must fit within a single word." (Answer 12-13). Appellant contends that such disclosure would not be a proper basis for the combination since there is no argument that such functionality would benefit Quach (Br. 16; Reply Br. 2). We agree with Appellant. While Hennessy describes the functions of bit fields, the Examiner has not shown how such information would have made the invention obvious to a person of ordinary skill in the art.

Similarly, the Examiner cites the teachings of Myers related to the effect of fatal errors on data integrity as the reason a person of ordinary skill in the art would have combined Quach and Hennessy (Answer 6). Appellant argues that such citation from Myers actually indicates that an opposite approach is taken in case of detecting a fatal error (Br. 21). We agree with Appellant. Myers, similar to Quach, does not redefine the error level and therefore, requires that the machine be shut down in case of fatal errors (FF 5 and 6).

Therefore, the specific solution and changes considered in each of the references results in different treatments of errors. Quach promotes/demotes the signaling mechanism and Myers shuts down and restarts the machine while Hennessy provides no information for redefining the error levels. In that regard, we find that the differences between these error handling approaches would not have prompted a person of ordinary skill in the relevant field to combine the elements in the way the instant claims require. Thus, we find that Examiner's rejection rests on speculation and less than a preponderance of the evidence and thus, fails to provide sufficient reasons for finding claims 10-13, 15-20, 22, and 23 unpatentable for obviousness under 35 U.S.C. § 103(a) over Quach and Hennessy and claims 1, 3, 4, and 6-9 over Quach, Hennessy, and Myers.

With respect to the rejections of the remaining claims over the combination of Quach, Hennessy, and Myers with Yamaguchi and Gervais, we note that the Examiner has not pointed to any teachings in these additional references that would have overcome the deficiency of the Quach, Hennessy, and Myers combination as discussed above. Thus, we do not

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sustain the 35 U.S.C. § 103 rejection of claims 14, 21, and 25 over Quach, Hennessy, and Yamaguchi, of claim 24 over Quach, Hennessy, and Gervais and of claim 5 over Quach, Hennessy, Myers, and Yamaguchi.

DECISION

The decision of the Examiner rejecting claims 1 and 3-25 under 35 U.S.C. § 103 is reversed.

REVERSED

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