

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte HIROO NAKANO

Appeal 2007-1984
Application 10/026,813¹
Technology Center 2100

Decided: November 7, 2007

Before ANITA PELLMAN GROSS, JEAN R. HOMERE,
and SCOTT R. BOALICK, *Administrative Patent Judges*.

BOALICK, *Administrative Patent Judge*.

DECISION ON APPEAL
STATEMENT OF THE CASE

This is an appeal under 35 U.S.C. § 134(a) from the final rejection of claims 1-4 and 11-14, all the claims pending in the application. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

¹ Application filed December 27, 2001. The real party in interest is Kabushiki Kaisha Toshiba.

Appellant's invention relates to a data processing apparatus that prevents the contents of data transferred to the data bus from being externally known through observation of a change in power consumption. (Spec. 1:16-18.) The apparatus includes a CPU (central processing unit), a memory, a pseudo-data generating circuit, and a data bus. (Spec. 4:4-11.) The pseudo-data generating circuit generates random number data which is output to the data bus as pseudo-data. (Spec. 7:21-25.)

Claim 1 is exemplary:

1. A data processing apparatus comprising:

an operation processing unit having at least a read cycle period when said operation processing unit reads data from a device, and a write cycle period when said operation processing unit writes data in the device;

a memory which performs data transmission/reception between said operation processing unit and said memory;

a data bus connected to said operation processing unit and said memory; and

a pseudo-data generating circuit connected to said data bus, said pseudo-data generating circuit which generates pseudo-data and outputs the pseudo-data to said data bus in a time interval between the read cycle period and the write cycle period, between the write cycle period and the read cycle period, between two read cycle periods, or between two write cycle periods.

The Examiner, in rejecting the claims, relies on the following prior art:

Feyt	US 6,698,662 B1	Mar. 2, 2004
Ugon	US 6,839,849 B1	Jan. 4, 2005

Claims 1-4 and 11-14 stand rejected under 35 U.S.C. § 103(a) as being obvious over Ugon and Feyt.

Rather than repeat the arguments of Appellant or the Examiner, we refer to the Brief and the Answer for their respective details. We have only considered in this decision those arguments that Appellant actually made in the Brief. Therefore, arguments not presented before us are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii) (2004).²

ISSUE

The issue is whether Appellant has shown that the Examiner erred in rejecting the claims under 35 U.S.C. § 103(a). The issue turns on whether Ugon and Feyt teach or suggest a pseudo-data generating circuit connected to a data bus which generates pseudo-data and outputs the pseudo-data to the data bus in a time interval between the read cycle period and the write cycle period, between the write cycle period and the read cycle period, between two read cycle periods, or between two write cycle periods.

² Except as will be noted in this opinion, Appellant has not presented any substantive arguments directed separately to the patentability of the dependent claims or related claims in each group. In the absence of a separate argument with respect to those claims, they stand or fall with the representative independent claim. *See* 37 C.F.R. § 41.37(c)(1)(vii).

FINDINGS OF FACT

The record supports the following findings of fact (FF) by a preponderance of the evidence.

1. Ugon describes a smart integrated circuit that includes a main processor 1 and a secondary processor 2, where each processor 1, 2 is connected by a data bus 3, 4 to working registers 11, 21 such as volatile RAMs and to memories 12, 13, 22 containing a main program P1 to be executed by the main processor 1 and a secondary program P2 to be executed by the secondary processor 2. (Col. 5, ll. 3-10.) Common power supply circuits 6 feed the two processors 1, 2, the busses 3, 4, and the memories 11, 21; 12, 13, 22. (Col. 6, ll. 18-22.)
2. Ugon teaches that the memories 21, 22 connected to the secondary processor 2 are "dummy" RAMs 21 and ROMs 22 that allow the secondary processor 2 to execute tasks that are superimposed on tasks of the main processor 1. (Col. 5, ll. 11-15.) The "dummy" memory of the secondary processor "does not play any real functional role" (col. 8, ll. 17-19) and "[t]he content of the 'dummy' RAM is of no functional importance, since it is used only to scramble the traces of the power consumption in the memory array" (col. 11, ll. 9-11). Ugon teaches that "[t]he signatures of the instructions used in the secondary processor are capable of concealing the effect of the signatures of the instructions executed in the main processor." (Col. 10, ll. 60-62.) The secondary program can "execute tasks without any correlation to the

- main program, or even incoherent tasks" for the purpose of hiding the functions of the main program. (Col. 10, l. 63 to col. 11, l. 3.)
3. Ugon teaches that the programs P1, P2 executed on the two processors 1, 2 may be executed simultaneously or that it is possible to phase shift the clock that controls the secondary processor 2 such that the instruction cycles do not exactly correspond in each of the processors 1, 2. (Col. 8, ll. 5-10.) The phase shift of the secondary processor 2 clock can be made variable and random. (Col. 8, ll. 10-12.)
 4. Ugon teaches that the two processors 1, 2 can communicate through a specific link, through a set of communication registers 50, 51 connected to the bus 3, 4, by cycle stealing through the bus of the other processor, or through arbitration logic in the case of a bus that is shared between the two processors. (Col. 7, ll. 11-16.) One embodiment of Ugon teaches that both the main processor 1 and the secondary processor 2 are connected to a common bus (col. 4, ll. 23-29; col. 7, ll. 14-16; col. 11, ll. 38-64; Fig. 3).
 5. Ugon also teaches an embodiment where the main processor 1 activates a timer R3 initialized either by the random generator R1 or from the content of nonvolatile memory 13. (Col. 11, ll. 13-16.) The timer R3 runs out at the end of a period that cannot be predicted from the outside and this triggers an authentication of the secondary processor 2 by the main processor 1. (Col. 11, ll. 18-21.) In another

embodiment, the register R2 can be used to trigger an interrupt after being loaded with particular information. (Col. 11, ll. 22-25.) In yet another embodiment, a random generator R1 is connected to the interrupt system 15 of the main processor 1 to generate interrupts that are irregular and not synchronized to the execution of programs in the main processor 1. (Col. 11, ll. 26-30.)

6. Feyt describes a device for hiding operations performed in a microprocessor card from analysis of the current consumed by the card. (Abstract.) In one embodiment, Feyt teaches masking the current consumption footprint of a cryptographic calculation (or other operation to be protected) by writing random data to a given part 26 of an EEPROM memory 14 reserved for that function. (Col. 3, ll. 34-54; Abstract; Fig. 3). Among other things, a random data item is presented on the data bus (step 2) prior to effecting the cryptographic calculation (step 5). (Col. 3, ll. 42, 45.)

PRINCIPLES OF LAW

All timely filed evidence and properly presented arguments are considered by the Board in resolving an obviousness issue on appeal. *See In re Piasecki*, 745 F.2d 1468, 1472 (Fed. Cir. 1984).

"Section 103 forbids issuance of a patent when 'the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.'" *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727,

1734 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, and (3) the level of skill in the art. *Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966). The Court in *Graham* further noted that evidence of secondary considerations, such as commercial success, long felt but unsolved needs, failure of others, etc., "might be utilized to give light to the circumstances surrounding the origin of the subject matter sought to be patented." 383 U.S. at 17-18.

In *KSR*, the Supreme Court emphasized "the need for caution in granting a patent based on the combination of elements found in the prior art," *id.* at 1739, and reaffirmed principles based on its precedent that "[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results," *id.*

ANALYSIS

Appellant contends that Examiner erred in rejecting claims 1-4 and 11-14 as being obvious over Ugon and Feyt. Reviewing the documents of record and the findings of facts cited above, we do not agree.

Regarding claim 1, Appellant argues that Ugon does not disclose a pseudo-data generating circuit which generates and outputs pseudo-data to a data bus. (Br. 12.) We do not agree.

The Examiner found that Ugon teaches "[a] pseudo-data generating circuit connected to said data bus (col. 11, lines 14-18), said pseudo-data generating circuit which generates pseudo-data and outputs the pseudo-data to said memory to cause instruction [sic] to randomly execute (col. 11, lines

22-25)." (Ans. 3.) Responding to the Examiner's findings, Appellant argues that "[a]t column 11, lines 14-18, Ugon describes outputs from a random generator (R1), a register (R2), and a timer (R3) that are supplied to a CPU 1 through an interrupt system 15. However, the outputs from the generator (R1), the register (R2) and the timer (R3) are not supplied to a bus (3,4)." (Br. 12.) We agree with Appellant on the narrow point that the precise portions of Ugon cited by the Examiner do not teach a pseudo-data generating circuit which generates and outputs pseudo-data to a data bus. (FF 5.)

This, however, does not end the matter because we find that Ugon elsewhere teaches a "pseudo-data generating circuit" as claimed. In particular, the second processor 2 of Ugon generates pseudo-data (FF 2) and outputs the pseudo-data to the data bus 4 (FF 1-2). Ugon also teaches that the main processor and the secondary processor 2 may share a common bus. (FF 4.)

As the Examiner correctly found, Feyt teaches that pseudo-data may be written to a data bus in a time interval between the read cycle period and the write cycle period, between the write cycle period and the read cycle period, between two read cycle periods, or between two write cycle periods. (Ans. 5; FF 6.) Moreover, Ugon discloses that the programs P1, P2 executed on the two processors 1, 2 may be executed simultaneously or it is possible to phase shift the clock that controls the secondary processor 2 so that the instruction cycles do not exactly correspond (FF 3). Therefore, by teaching that the clock controlling the secondary processor 2 can be phase shifted with respect to the main processor 1, Ugon also teaches one of ordinary skill in the art that the pseudo-data may be written to the data bus by the

secondary processor 2 in a time interval between the read cycle period and the write cycle period, between the write cycle period and the read cycle period, between two read cycle periods, or between two write cycle periods of the main processor 1.

Thus, we conclude that the subject matter of claim 1 would have been obvious to one of ordinary skill in the art given the combined teachings of Ugon and Feyt, or given Ugon alone.

We have considered Appellant's remaining arguments and find them unpersuasive. Accordingly, we conclude that the Examiner did not err in rejecting claim 1 under 35 U.S.C. § 103(a). Claims 2-4 and 11-14 were not argued separately, and fall together with claim 1.

NEW GROUND OF REJECTION UNDER 37 C.F.R. § 41.50(b)

Because our decision relies at key points on different reasoning with respect to the Ugon patent than was set forth by the Examiner, we designate our decision as a new ground of rejection under 37 C.F.R. § 41.50(b).

37 C.F.R. § 41.50(b) provides that a "new ground of rejection pursuant to this paragraph shall not be considered final for judicial review."

37 C.F.R. § 41.50(b) also provides that the Appellant, *WITHIN TWO MONTHS FROM THE DATE OF THE DECISION*, must exercise one of the following two options with respect to the new grounds of rejection to avoid termination of proceedings (37 C.F.R. § 1.197 (b)) as to the rejected claims:

- (1) Reopen prosecution. Submit an appropriate amendment of the claims so rejected or new evidence relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the proceeding will be remanded to the examiner ...

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(2) Request rehearing. Request that the proceeding be reheard under 37 C.F.R. § 41.52 by the Board upon the same record ...

CONCLUSION OF LAW

Based on the findings of facts and analysis above, we conclude that:

- (1) The Examiner did not err in rejecting claims 1-4 and 11-14 for obviousness under 35 U.S.C. § 103.
- (2) Claims 1-4 and 11-14 are not patentable.

DECISION

The rejection of claims 1-4 and 11-14 for obviousness under 35 U.S.C. § 103 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED
37 C.F.R. § 41.50(b)

KIS

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