

The opinion in support of the decision being entered today is
not binding precedent of the Board

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SHENQING FANG, TIMOTHY THURGATE,
KUO-TUNG CHANG, RICHARD FASTOW,
ANGELA T. HUI, KAZUHIRO MIZUTANI,
KELWIN KO, HIROYUKI KINOSHITA
YU SUN and HIROYUKI OGAWA

Appeal 2007-2105
Application 10/762,445
Technology Center 2800

Decided: August 17, 2007

Before JOSEPH F. RUGGIERO, MAHSHID D. SAADAT,
and ROBERT E. NAPPI, *Administrative Patent Judges*.

SAADAT, *Administrative Patent Judge*.

DECISION ON APPEAL
STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134(a) from the Examiner's
Final Rejection of claims 1, 2, 4-9, and 11-14, which are all of the claims

pending in this application as claims 3 and 10 have been canceled. We have jurisdiction under 35 U.S.C. § 6(b).

Appellants' invention relates to a floating gate flash memory cell having reduced drain induced barrier lowering (DIBL) and a sufficiently low V_{ss} resistance (Specification 2). Appellants provide for a recess formed in the substrate adjacent to a stacked gate structure of the memory cell, where the recess has a sidewall, a bottom, and a depth (Specification 3). The source region is formed adjacent to the sidewall of the recess and under the stacked gate structure while a V_{ss} connection region is formed under the bottom of the recess and under the source and connected to the source (*id.*). According to Appellants, the V_{ss} connection region under the bottom of the recess, in addition to having a reduced resistance, reduces the DIBL by lowering the lateral diffusion of the source in the channel region (Specification 3-4).

Independent Claim 1 is representative and reads as follows:

1. A floating gate memory cell situated on a substrate, said floating gate memory cell comprising:

a stacked gate structure situated on said substrate, said stacked gate structure being situated over a channel region in said substrate;

a recess formed in said substrate adjacent to said stacked gate structure, said recess having a sidewall, a bottom, and a depth;

a source of said floating gate memory cell situated adjacent to said sidewall of said recess and under said stacked gate structure;

a V_{ss} connection region situated under said bottom of said recess and under said source, said V_{ss} connection region being

connected to said source, said Vss connection region being a heavily doped region to reduce a Vss resistance;

wherein said Vss connection region being situated under said bottom of said recess causes said source to have a reduced lateral diffusion in said channel region, thereby preventing an increase in a drain induced barrier lowering.

The Examiner relies on the following prior art in rejecting the claims:

Hori	US 6,147,379	Nov. 14, 2000
Kobayashi	US 6,721,205 B2	April 13, 2004 (filed Dec. 14, 2000)

The Examiner rejected claims 1, 2, 4-6, 8, 9, and 11-13 under 35 U.S.C. § 102(b) as anticipated by Hori and Kobayashi¹ and claims 7 and 14 under 35 U.S.C. § 103(a) as being unpatentable over Hori and Kobayashi.

Rather than repeat the arguments here, we make reference to the Brief and the Answer for the respective positions of the Appellants and the Examiner.

We reverse.

ISSUE

Appellants and the Examiner disagree as to whether Hori discloses the recited source and Vss connection regions such that the resulting reduced lateral diffusion of the source prevents an increase in a drain induced barrier

¹ Although the Examiner has based the anticipation rejection of the claims on both Hori and Kobayashi (Answer 3), it appears that the Examiner intended to rely on Kobayashi to show that Hori's bit line connection is inherently the same as the Vss connection (Answer 9). Therefore, for the purpose of this appeal, we consider the rejection to be based only on Hori.

lowering. Appellants contend that Hori not only increases the electric field adjacent to the drain, which teaches away from reducing the DIBL problem, but also fails to show a V_{ss} connection region under the source region (Br. 8). The Examiner contends that the bit line or the V_{ss} connection region in Hori is “under the bottom of the recess (14) and under the source 7b” (Answer 9). The Examiner further asserts that since the V_{ss} region is fully recessed in relation to the source region, it will reduce the DIBL (Answer 10).

The issue, therefore, is whether the Examiner erred in rejecting the claims under 35 U.S.C. §§ 102(e) and 103(a). The issue specifically turns on whether Hori anticipates Appellants’ claimed invention by disclosing a V_{ss} connection region situated under the bottom of the recess and under the source of a floating gate memory cell.

FINDINGS OF FACT

The following findings of fact (FF) are relevant to the issue involved in the appeal and are believed to be supported by a preponderance of the evidence.

1. Hori relates to nonvolatile semiconductor memory devices (Abstract) wherein a stacked floating gate is positioned over a stepped channel region (col. 9, ll. 5-17).
2. As depicted in Figure 1A, source region 7 includes a high-concentration impurity layer 7a and a low-concentration impurity layer 7b (col. 9, ll. 64-66).
3. The low-concentration impurity layer 7b is provided between the high-concentration impurity layer 7a and the channel region 9 and faces

an edge portion of the floating gate 4 via the tunnel oxide film 3 (col. 10, ll. 1-5).

4. Hori further shows that the source region 7 is connected to a bit line (fig. 1A; col. 10, ll. 5-6).

5. Hori refers to the high-concentration impurity layer 7a and the low-concentration impurity layer 7b of the source region 7 as a high-concentration source region 7a and a low-concentration source region 7b, respectively (col. 10, ll. 6-11).

6. In a plan view of the memory cell depicted in Figure 1B, Hori shows the regions of high and low concentration source 7a and 7b as well as drain 8a and 8b in relationship with the floating gate (col. 10, ll. 24-46).

PRINCIPLES OF LAW

A rejection for anticipation requires that the four corners of a single prior art document describe every element of the claimed invention, either expressly or inherently, such that a person of ordinary skill in the art could practice the invention without undue experimentation. *See Atlas Powder Co. v. IRECO, Inc.*, 190 F.3d 1342, 1347, 51 USPQ2d 1943, 1946 (Fed. Cir. 1999); *In re Paulsen*, 30 F.3d 1475, 1478-79, 31 USPQ2d 1671, 1673 (Fed. Cir. 1994).

ANALYSIS

As described above, the source region of Hori includes a low concentration region 7b and a high concentration region 7a. The Examiner's characterization of the high concentration region 7a as the V_{ss} appears to

remain undisputed by Appellants. However, Appellants argue that the Vss connection region is at the same elevation level as the low concentration source 7b and therefore, does not meet the claim language (Br. 8). The Examiner responds by stating that “a small part of Hori’s ‘Vss connection region’ 7a is situated under the bottom of the recess (14) and under the source 7b” (Answer 9).

The memory cell disclosed by Hori includes a low concentration source area that is positioned under the edge of the stacked gate between the channel area and the high concentration source area (FF 1-3). The memory cell further includes a high concentration source area which is shown in Figure 1A as being between the low concentration source 7b and the recess edge 15. Source 7a further extends to an area under the recess bottom 14. The source region that is connected to the bit line or the Vss, as asserted by the Examiner, is actually the high concentration area 7a (FF 4). Therefore, while Hori refers to both regions 7a and 7b as “source” (FF 5-6); we agree with the Examiner to the extent that Hori shows the Vss connection region under the bottom of the recess.

However, as argued by Appellants (Br. 8), a portion of the Vss connection region is adjacent to the recess wall and is positioned on the top surface of the semiconductor substrate at the same elevation level as source 7b extending to an area near the floating gate stack (FF 6). In the specific configuration of the Vss connection region disclosed in Hori, the region that is situated adjacent to the sidewall of the recess is the Vss connection region, and not the source, as required by the claim. Additionally, although it may be situated below the source level, the Vss connection region situated under

the bottom of the recess is not under the source region. The Vss connection region under the bottom of the recess, at best, is under the remaining part of the Vss connection region that continues at the recess wall towards the gate stack. The only positional relationship between the source and the Vss connection region disclosed in Hori is that the source is between the Vss connection region and the channel region (FF 3). This configuration results in the Vss connection region being adjacent, and not under the source, as required by the claims.

CONCLUSION

On the record before us, we find that the Examiner fails to make a prima facie case that Hori anticipates claim 1 or the other independent claim 8, which includes similar limitations. Therefore, in view of our analysis above, the 35 U.S.C. § 102 rejection of claims 1, 2, 4-6, 8, 9, and 11-13 as anticipated by Hori cannot be sustained. Additionally, we do not sustain the 35 U.S.C. § 103 rejection of claims 7 and 14 over Hori and Kobayashi as the Examiner has not identified any teachings in Kobayashi related to the Vss connection region situated under the source to overcome the deficiencies of Hori discussed above.

DECISION

The decision of the Examiner rejecting claims 1, 2, 4-6, 8, 9, and 11-13 under 35 U.S.C. § 102 and claims 7 and 14 under 35 U.S.C. § 103 is reversed.

Appeal 2007-2105
Application 10/762,445

REVERSED

eld

FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO CA 92691