

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SHARON M. EBNER and JOHN A. WICKERAAD

Appeal 2007-2216
Application 09/560,908
Technology Center 2100

Decided: January 3, 2008

Before JOHN C. MARTIN, ANITA PELLMAN GROSS,
and JEAN R. HOMERE, *Administrative Patent Judges*.

HOMERE, *Administrative Patent Judge*.

DECISION ON APPEAL
STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134 from the Examiner's final rejection of claims 3 through 7, 10 through 15, 17 through 21, 23 through 28 and 30 through 34. Claims 1, 2, 8, 9, 16, 22, and 29 have been canceled. We have jurisdiction under 35 U.S.C. § 6(b). We affirm.

The Invention

Appellants invented a method and system for reading and writing cache status information in a cache memory. Particularly, the invention allows one or more requesters to read and write cache status information (preferably concurrently) from a status data table stored in a multi-port memory. (Spec. 5.)

An understanding of the invention can be derived from exemplary independent claims 3 and 17, which read as follows:

3. A method of providing cache status information of a plurality of cache lines in a cache memory, comprising:

providing a cache status data table having a plurality of status entries, each of said plurality of status entries corresponding to one of said plurality of cache lines in said cache memory, and each of said plurality of cache status entries having a plurality of cache status bits that indicates status of said corresponding one of said plurality of cache lines;

storing said cache data status table in a multi-port memory having one or more read ports configured to allow one or more requestors to read said plurality of cache status entries and one or more write ports configured to allow said one or more requestors to write to said plurality of cache status entries;

receiving a first cache entry line number corresponding to a first one of said plurality of cache lines from a first requestor at said multi-port memory;

allowing said first requestor an access to a first requested one of said plurality of status entries that corresponds to said first cache entry line number; and

accessing a first cache line of said cache memory corresponding to said first cache entry line number based on said first requested one of said plurality of status entries by said first requestor.

17. A cache memory system, comprising:¹

a cache memory having a plurality of cache lines;

a cache status data table having a plurality of status entries, each of said plurality of status entries corresponding to one of said plurality of cache lines in said cache memory, and each of said plurality of cache status entries having a plurality of cache status bits that indicates status of said corresponding one of said plurality of cache lines; and,

a multi-port memory for storing said cache data status table separate from said cache memory, said multi-port memory having one or more read ports and one or more write ports configured to concurrently allow one or more requestors to concurrently write to and read from said plurality of cache status entries, wherein a requestor accesses one of said plurality of status entries by a cache entry line number and said requestor accesses a cache line of said cache memory corresponding to said cache entry line number based on said one of said plurality of status entries by said requestor.

The Examiner relies upon the following prior art to reject the claims on appeal,

McClure	US 5,513,335	Apr. 30, 1996
Arimilli	US 5,613,153	Mar. 18, 1997
Byrn	US 5,761,716	Jun. 2, 1998
Camacho	US 6,167,487	Dec. 26, 2000

The Examiner rejects the claims on appeal as follows:

A. Claims 3 through 7 and 10 through 13 stand rejected under 35 U.S.C. § 102(b) as being anticipated by McClure.

¹ Claim 17 as reproduced in the Claims Appendix (App. Br. 28) includes an error: It omits “entries” in line 5 of the third paragraph of the claim as reproduced herein.

- B. Claim 14 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of McClure and Arimilli.
- C. Claim 15 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of McClure, Arimilli, and Byrn.
- D. Claims 17, 18, 21, 23 through 28, and 30 through 33 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of McClure and Camacho.
- E. Claims 19 and 34 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of McClure, Camacho, and Arimilli.
- F. Claim 20 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of McClure, Camacho, Arimilli, and Byrn.

FINDINGS OF FACT

The following findings of fact are supported by a preponderance of the evidence.

The Invention

1. Appellants invented a method and system for allowing one or more requesters (103) to read and write cache status information from a status data table² (200) stored in a cache status block (101), which includes a multi-port memory.³ (Spec. 5.)

² The status data table (200) includes a plurality of status entries corresponding to cache lines in a cache memory (102). The status data table further includes a plurality of cache status entries (201-211) having a plurality of status bits indicating the corresponding status of each of the cache lines. Further, each status entry includes status bits indicating the types of ownership (e.g., shared or private) of the corresponding cache line. (Spec. 6.)

2. As depicted in Figures 1 through 3, upon receiving an entry line number (107) from a requester (103), the cache status block (101) locates the requested line entry in the status data table (200). (*Id.* 6.)

The Prior Art Relied Upon

3. As shown in Figure 2, McClure discloses a cache tag RAM (34) that communicates with a data cache (32), a local processor (36), and a system bus (26). (Col. 3, ll. 35-42.)

4. As depicted in Figure 4, the tag RAM (34) includes a first single-port memory array (40) dedicated to the local processor (36) for reading and writing via the first port. The RAM (34) also includes a second single-port memory array (44) dedicated to the system memory for reading and writing via the second port. Both the first and second ports operate asynchronously relative to each other. Further, the RAM (34) includes a dual-port memory array (48) that stores information or status bits about the cache memory, wherein the stored entries are shared by both the first and second single-port memory arrays (40, 44). (Abstract, and col. 4, ll. 1-5, ll. 34-42, col. 5, ll. 22-30.)

5. McClure discloses that upon a receiving address and control signals from the local processor (36) to access a designated status entry in the dual-port memory array (48), the first single port (40) locates the requested status entry in the dual-port memory array (48). Similarly, the

³ The multi-port memory may include a number of read ports and a number of write ports to allow several requesters to concurrently access cache status data information from a cache status block (Spec. 5:21-24).

second single-port array (44) uses received address and control signals to locate the designated status entry from the dual-port memory. (Col. 3, ll. 52-59, col. 4, ll. 34-42.) These address signals include the “LSB Local Address” and “LSB System Address” information depicted in Figure 3 (col. 3, ll. 43-44 and 60-61).

6. McClure further discloses that the status bits stored in the dual-port memory array (48) include a snoop valid bit, parity bits, or bits required by the MOESI protocol. MOESI stands for Modified, Owned, Exclusive, Shared, and Invalid, and is utilized to indicate cache states. (Col. 4, ll. 5-9.)

7. As depicted in Figure 5, Arimilli discloses that direct memory access (DMA) data caches are known to have status bits that traditionally support the Modified, Exclusive, Shared, Invalid states according to the MESI protocol. (Col. 5, ll. 28-35.)

8. Byrn discloses a mechanism for monitoring the space availability in a cache. Particularly, Byrn discloses a time stamp mechanism for indicating the last time a cache block was accessed. (Col. 8, ll. 21-29.)

9. Camacho teaches a multi-port RAM that allows concurrent read and write accesses from different ports. (Col. 1, ll. 65-67.)

PRINCIPLES OF LAW

1. ANTICIPATION

It is axiomatic that anticipation of a claim under § 102 can be found only if the prior art reference discloses every element of the claim. *See In re King*, 801 F.2d 1324, 1326 (Fed. Cir. 1986) and *Lindemann*

Maschinenfabrik GMBH v. American Hoist & Derrick Co., 730 F.2d 1452, 1458, 221 USPQ 481, 485 (Fed. Cir. 1984).

In rejecting claims under 35 U.S.C. § 102, a single prior art reference that discloses, either expressly or inherently, each limitation of a claim invalidates that claim by anticipation. *Perricone v. Medicis Pharmaceutical Corp.*, 432 F.3d 1368, 1375-76 (Fed. Cir. 2005) (citing *Minn. Mining & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc.*, 976 F.2d 1559, 1565 (Fed. Cir. 1992)). Anticipation of a patent claim requires a finding that the claim at issue “reads on” a prior art reference. *Atlas Powder Co. v. IRECO, Inc.*, 190 F.3d 1342, 1346 (Fed. Cir. 1999) (“In other words, if granting patent protection on the disputed claim would allow the patentee to exclude the public from practicing the prior art, then that claim is anticipated, regardless of whether it also covers subject matter not in the prior art.”) (internal citations omitted).

2. OBVIOUSNESS (Prima Facie)

The Supreme Court in *Graham v. John Deere Co.*, 383 U.S. 1, 17-18, (1966), stated that the following factual inquiries underpin any determination of obviousness:

Under § 103, [1] the scope and content of the prior art are to be determined; [2] differences between the prior art and the claims at issue are to be ascertained; and [3] the level of ordinary skill in the pertinent art resolved. Against this background, the obviousness or nonobviousness of the subject matter is determined. Such [4] secondary considerations as commercial success, long felt but unsolved needs, failure of others, etc., might be utilized to give light to the circumstances surrounding the origin of the subject matter sought to be patented. As

indicia of obviousness or nonobviousness, these inquiries may have relevancy.

Where the claimed subject matter involves more than the simple substitution one known element for another or the mere application of a known technique to a piece of prior art ready for the improvement, a holding of obviousness must be based on “an apparent reason to combine the known elements in the fashion claimed.” *KSR Int’l v. Teleflex, Inc.*, 127 S. Ct. 1727, 1740-41 (2007). That is, “there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *Id.* at 1741 (quoting *In re Kahn*, 441 F.3d at 988). Such reasoning can be based on interrelated teachings of multiple patents, the effects of demands known to the design community or present in the marketplace, and the background knowledge possessed by a person having ordinary skill in the art. *KSR*, 127 S. Ct. at 1740-41.

ANALYSIS

A. 35 U.S.C § 102(b) REJECTION

Claims 3 through 7 and 10 through 13

As detailed in the Findings of Fact (FF) section above, McClure discloses a dual-port memory array 48 that stores status bits for the cache memory. (FF 4.) McClure also discloses a first single-port memory array 40 and a second single-port memory array 44 for locating in the dual-port memory array cache status entries designated by the processor and the system bus. (FF 5.) Additionally, McClure discloses that the dual-port memory array and the two single-port memory arrays, together, form a cache

tag RAM 34 that communicates with the local processor, the data cache, and the system bus. (FF 3.)

The limitation at issue in independent claim 3 is “receiving a first cache entry line number corresponding to a first one of a plurality of cache lines from a first requestor at a multi-port memory.” (App. Br. 23.) We agree with the Examiner that McClure reasonably teaches this limitation. The Examiner found (Ans. 24, last two lines), and Appellant does not dispute, that the “LSB Local Address” and the “LSB System Address” each can be characterized as a “cache line entry number.” Thus, the sole issue before us regarding claim 3 is whether these cache line numbers are received “at a multi-port memory.”

The Examiner reads the recited “multi-port memory” on McClure in two alternative ways: (1) on RAM 34 (i.e., on the combination of single-port memory array 40, dual-port memory array 48, and single-port memory array 44); and (2) on dual-port memory 48 alone. (Ans. 24-27.) We begin by considering the scope and meaning of “multi-port memory,” which must be given its broadest reasonable interpretation consistent with Appellants’ disclosure, as explained in *In re Morris*, 127 F.3d 1048 (Fed. Cir. 1997):

[T]he PTO applies to the verbiage of the proposed claims the broadest reasonable meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art, taking into account whatever enlightenment by way of definitions or otherwise that may be afforded by the written description contained in the applicant's specification.

Id. at 1054. The Specification explains that “in a preferred embodiment of the present invention, the cache status block 101 comprises a multi-port memory device having any number of read ports and write ports to enable

several requesters to concurrently access the cache status information from the cache status block 101.” (Spec. 5:21-24.) We do not understand this passage to be a definition of “multi-port memory” and thus as requiring the ability to permit concurrent access by several requestors. Nor do Appellants so contend, instead reserving their arguments about concurrent access to independent claim 17, which expressly requires that the recited “multi-port memory” be capable of providing concurrent access (Br. 16).

The Examiner, on the other hand, argues that a multi-port memory necessarily is capable of providing concurrent access, citing the definition of Subclass 149 (“Multiport memory”) of Class 711.⁴ That subclass definition reads: “[s]ubject matter including means or steps for controlling shared memory capable of supporting a plurality of simultaneous read accesses” (Ans. 25). We agree with Appellants (Reply Br. 4) that the Examiner’s reliance on this definition is misplaced. We are not persuaded that this subclass definition represents the broadest reasonable interpretation of “multiport memory” that would have been accorded that term by persons having ordinary skill in the art. Instead, the definition represents PTO classification considerations that may or may not reflect the customary and ordinary meaning of “multiport memory.”

In the absence of a controlling definition to the contrary, we conclude that the term “multi-port memory” as used in Appellants’ claims is broad enough to read on a memory that has plural ports for writing to and/or reading from the memory.

⁴ The title of Class 711 is “Electrical Computers and Digital Processing Systems: Memory.”

In response to the Examiner's position that "multi-port memory" can be read on RAM 34, i.e., on single-port memory arrays 40 and 44 and dual-port memory array 48, Appellants argue that this position

is unreasonable, at odds with generally accepted use of the term in the electronic arts, and, importantly, is inconsistent with the usage of such terms in the cited art, e.g., McClure and Camacho. McClure clearly identifies memories 40 and 44 as being single port memories, and differentiates them from dual port memory 48. Notably, McClure does not identify the composite structure comprising multiple memory structures 40, 44 and 48, collectively "cache tag RAM 34," as a multi-port memory. Further, McClure has an extensive discussion (McClure column 4 lines 13-33 and column 2 lines 19-24) on the basis for selecting a combination of single and dual (multi) port structures.

(Br. 9-10.) In the discussion to which Appellants refer, McClure explains that a "dual-port memory array" can be two and one-half to three and one-half times or more larger than a "single-port memory array" (col. 4, ll. 13-33). While it is true that McClure does not characterize RAM 34, i.e., the combination of memory arrays 40, 44, and 48, as a "multi-port memory," nothing in McClure suggests it would be unreasonable to apply the term "multi-port memory" to the combination of those memory arrays. Nor have Appellants cited any definition that restricts the term "memory" to a single memory array. Appellants therefore have not shown that the Examiner erred in finding that RAM 34 is a dual-port memory. Inasmuch as a cache entry line number in the form of the "LSB Local Address"⁵ is applied to one port of RAM 34, while a cache line entry number in the form of "LSB System

⁵ As already noted, Appellants do not deny that these LSBs can accurately be characterized as cache entry line numbers.

Address” is applied to the other port of RAM 34, the cache line numbers are received “at a multi-port memory,” as required by claim 3.

Thus, Appellants have not shown error in the Examiner’s position that claim 3 is anticipated by McClure when the recited “multi-port memory” is read on McClure’s RAM 34, i.e., the combination of single-port memory arrays 40 and 44 and dual-port memory array 48.

There is also merit in the Examiner’s alternative position that anticipation exists even if the recited “multi-port memory” is read on only McClure’s “dual-port” memory array 48 (Ans. 26). Appellants argue that anticipation is lacking because “memory 48 . . . does not receive a cache line entry number (address)” (Reply Br. 1), as required by claim 3 (“receiving a first cache entry line number . . . at a multi-port memory”). Instead, Appellants contend, the LSBs are received by the single-port memory arrays and do not reach the dual-port memory array (*id.* at 3). The Examiner found that these LSBs are inherently passed through the single-port memory arrays to dual-port memory array 48:

Although not explicitly recited by McClure that the LSB is received at the dual-port memory array, the teachings of McClure do not provide for another way of indexing the dual-port memory array in order to retrieve status bits without the passing through of the LSB (cache entry line number) from the single port-memories [sic; single-port memories] (40,44) to the dual-port memories (col. 5, lines 24-30). This is especially evident as shown in Figure 4, which shows the dual-port memory with two other output lines (labeled as 56, which pass the snoop valid bit), and one other input port for passing the output of logical gate 64. Thus, this output of the AND gate 64 is unable to transmit the LSB (cache entry line number) to the dual-port memory, and although not explicitly recited by McClure, there is no other way of indexing the dual-port

memory array in order to retrieve status bits without the passing through of the LSB (cache entry line number) from the single port-memories [sic] (40,44) to the dual-port memories.

(Ans. 24.) This reasoning is persuasive and sufficient to prima facie establish inherency, thereby shifting the burden of persuasion on that issue to Appellants. *In re Schrieber*, 128 F.3d 1473, 1478 (Fed. Cir. 1997). Appellants have not met this burden. Rather than positing at least one way that memory 48 can access the required status information without receiving the LSBs (or other data derived therefrom representing a cache entry line number), Appellants simply argue that the Examiner failed to make out a prima facie case for inherency.

Appellants have therefore also failed to show error in the Examiner's finding that the subject matter of claim 3 is prima facie anticipated by McClure when the recited "multi-port memory" is read on only dual-port memory array 48.

Accordingly, we are affirming the rejection of claim 3 for anticipation by McClure.

Appellants did not provide separate arguments with respect to the rejection of claims 4 through 7 and 10 through 13. Therefore, we select independent claim 3 as being representative of the cited claims. These claims consequently fall together with representative claim 3. *See In re Young*, 927 F.2d 588, 590 (Fed. Cir. 1991). *See also* 37 C.F.R. § 41.37(c)(1)(vii).

B. 35 U.S.C. § 103(a) REJECTIONS

Claims 14 and 15

First, we note that Appellants repeat for claims 14 and 15, which depend on independent claim 10 through claim 13, the same arguments that we addressed above in our discussion of independent claims 3 and 10. As discussed above, we find that McClure teaches the claimed multi-port memory that receives a first entry line number corresponding to a first one of a plurality of cache lines.

Claim 14 further requires that the cache status bits include “one or more bits indicating a type of ownership of said owner of said corresponding one of said plurality of cache lines” and “one or more bits indicating whether a direct memory access operation involving said corresponding one of said plurality of cache lines is pending.” The Examiner found that McClure discloses “type of ownership” status bits and relies on Arimilli for DMA access status bits. (Ans. 10.) As Appellants do not challenge the Examiner’s reliance on Arimilli for DMA status bits, we only need to consider whether McClure as modified in view of Arimilli would include “type of ownership” status bits.

Appellants contend that McClure and Arimilli both are silent with respect to the “type of ownership” limitation (Br. 13). Specifically, Appellants reason that

McClure teaches a MOESI (modified, owned, exclusive, shared, invalid) protocol that may include information that a cache is owned (column 4, lines 5-8 of McClure). Similarly, Arimilli teaches a MESI (modified, exclusive, shared, invalid) protocol (column 5, lines 35-38 of Arimilli). However,

Arimilli's MESI protocol does not support information of ownership.

(Br. 13.) The Examiner correctly rejected Appellants' apparent position that the only "type of ownership" bit disclosed in McClure and Arimilli is the "O" (owned) bit in McClure's MOESI protocol. As explained by the Examiner, the "S" (shared) bit in the MOESI and MESI protocols represents type of ownership because it indicates that the same data exists in at least two memories and thus is owned by at least the controllers in those memories. (Ans. 28.) The Reply Brief fails to address or point out any error in this position of the Examiner. Appellants have therefore failed to show that the Examiner erred in rejecting dependent claim 14 as being unpatentable over the combination of McClure and Arimilli.

We also are affirming the rejection with respect to claim 15, whose own limitations are not separately argued.

Claims 17 through 21, 23 through 28, 30 through 34

First, we note that regarding independent claims 17, 21, and 28, Appellants reiterate the same arguments that we addressed above in our discussion of independent claim 3. As discussed above, we find that McClure teaches the claimed multi-port memory that receives a first entry line number corresponding to a first one of a plurality of cache lines.

Independent claim 17 further requires that the multi-port memory is "configured to concurrently allow one or more requestors to concurrently write to and read from said plurality of cache status entries."⁶ We agree

⁶ As noted above, the term "entries" is omitted from this language in the copy of this claim in the Claims Appendix.

with the Examiner that the combination of McClure and Camacho reasonably teaches that limitation.

McClure's cache tag RAM 34 includes a plurality of ports (a first single port and a second single port, both being able to perform read and write accesses) that allow one or more requestors (processor or system bus) to locate designated cache status entries from an array of cache status entries stored in the dual port memory. (FF 3-5.) Camacho discloses a multi-port RAM that allows one or more requestors to simultaneously perform read and write accesses from different ports. (FF 9.) The Examiner concluded that it would have been obvious to modify McClure's cache accessing system to include the simultaneous accessibility of Camacho since this would reduce the total processing time for read and write transactions in the resulting McClure-Camacho system. (Ans. 13.)⁷ Appellants responded as follows:

With respect to McClure, a given requestor does not have access to both single port memories (40, 44), and cannot concurrently read and write to the dual-port memory (48). Further, McClure actually teaches away from utilizing a multi-port memory in the manner of the recited limitation, teaching that a multi-port memory is undesirably large for this use (col. 4, lines 13-33). Camacho is silent with respect to use of a multi-port memory for cache. Consequently, Camacho does not overcome the deficiencies of McClure, and neither McClure nor Camacho, alone or in combination, teach, disclose or suggest the limitations of claims 17, 21, and 28.

⁷ Citing the aforementioned subclass definition of "multiport memory," the Examiner also held that McClure's dual-port memory is inherently capable of simultaneous access operations (Ans. 28). As explained above, the Examiner's reliance on that definition is misplaced.

(App. Br. 16.) These arguments are unpersuasive. While it is true that in McClure a given requestor (e.g., the local processor) cannot access both single-port memory arrays, this fact is not relevant to the propriety of the rejection. Claim 17 does not require access to plural ports by a single requester, instead specifying that the multi-port memory “ha[s] one or more read ports and one or more write ports configured to concurrently allow one or more requestors to concurrently write to and read from said plurality of cache status entries.” In McClure, considered both before and after modification in view of Camacho, the local processor has access (specifically, nonconcurrent access) to one port and the system bus has access to the other port. Furthermore, after modification in view of Camacho, the local processor and the system bus can have concurrent access to their respective ports, which is enough to satisfy the claim.

We also are not persuaded by the “teaching away” argument that “McClure actually teaches away from utilizing a multi-port memory in the manner of the recited limitation, teaching that a multi-port memory is undesirably large for this use (col. 4, lines 13-33).” The determination of obviousness must consider, *inter alia*, whether a person of ordinary skill in the art would have been motivated to combine the prior art to achieve the claimed invention and whether there would have been a reasonable expectation of success in doing so. *Brown & Williamson Tobacco Corp. v. Philip Morris, Inc.*, 229 F.3d 1120, 1124 (Fed. Cir. 2000). *Medichem S.A. v. Rolabo S.L.*, 77 USPQ2d 1865, 1869 (Fed. Cir. 2006). Where the teachings of two or more prior art references conflict, the Examiner must weigh the power of each reference to suggest solutions to one of ordinary skill in the

art, considering the degree to which one reference might accurately discredit another. *In re Young*, 927 F.2d 588, 591 (Fed. Cir. 1991). If the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 902 (Fed. Cir. 1984.) Furthermore, our reviewing court has held that “[a] reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant.” *In re Gurley*, 27 F.3d 551, 553 (Fed. Cir. 1994). *See also Para-Ordnance Mfg. v. SGS Importers Int’l*, 73 F.3d 1085, 1090 (Fed. Cir. 1995).

McClure’s silence with regard to permitting concurrent access to both single-port memories by the local processor and the system bus would not have been understood as discouraging the ordinarily skilled artisan from modifying McClure to provide that capability. Nor would such a modification have been discouraged by McClure’s disclosure that space can be saved by configuring RAM 34 as a combination of two single-port memories and a dual-port memory rather than as a dual-port memory (col. 4, ll. 13-33). We assume Appellants’ contention to the contrary is based on the incorrect assumption that the Examiner is proposing to replace all three of McClure’s single-port and dual-port memory arrays 40, 44, and 48 with Camacho’s dual-port memory array. However, we understand the Examiner’s position to be that it would have been obvious to modify McClure’s dual-port memory array 48 (and also the single-port memory

arrays, if necessary) to permit concurrent accessing by the local processor and the system bus. Appellants have not explained why such a modification of McClure would have been perceived as running counter to McClure's teachings about space savings.

Appellants' argument that "Camacho is silent with respect to use of a multi-port memory for cache" is not understood. While the term "cache" is not used in the "Best Mode for Carrying Out the Invention" section (cols. 3-8) of the Camacho's Specification, cache memory applications of the disclosed memory architecture are discussed in the "Disclosure of the Invention" section (cols. 1-3) and recited in Camacho's claims (e.g., claim 1).

For the foregoing reasons, the Examiner has not been shown to have erred in rejecting independent claim 17 as being unpatentable over the combination of McClure and Camacho.

Appellants did not provide separate arguments with respect to the other claims that stand rejected over the combination of McClure and Camacho, i.e., claims 18, 21, 23 through 28, and 30 through 33, which consequently fall together with representative claim 17. *See* 37 C.F.R. § 41.37(c)(1)(vii).

Appellants also failed to separately argue the merits of dependent claims 19, 20, and 34, which stand rejected over McClure and Camacho in view of other references. Those claims therefore fall with their parent claims.

SUMMARY

Appellants have not shown that the Examiner failed to establish that:

- A. Claims 3 through 7 and 10 through 13 are anticipated by McClure under 35 U.S.C. § 102(b).
- B. Claim 14 is unpatentable over the combination of McClure and Arimilli under 35 U.S.C. § 103(a).
- C. Claim 15 is unpatentable over the combination of McClure, Arimilli, and Byrn under 35 U.S.C. § 103(a).
- D. Claims 17, 18, 21, 23 through 28, and 30 through 33 are unpatentable over the combination of McClure and Camacho under 35 U.S.C. § 103(a).
- E. Claims 19 and 34 are unpatentable over the combination of McClure, Camacho, and Arimilli under 35 U.S.C. § 103(a).
- F. Claim 20 is unpatentable over the combination of McClure, Camacho, Arimilli, and Byrn under 35 U.S.C. § 103(a).

DECISION

We affirm the Examiner's decision rejecting claims 3 through 7, 10 through 15, 17 through 21, 23 through 28, and 30 through 34.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

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Appeal 2007-2216
Application 09/560,908

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