

The opinion in support of the decision being entered today
is *not* binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Ex parte CHRIS BALDWIN

Appeal 2007-2342
Application 10/884,654
Technology Center 2800

Decided: July 12, 2007

Before ERIC GRIMES, NANCY J. LINCK, and
RICHARD M. LEBOVITZ, *Administrative Patent Judges*.

LEBOVITZ, *Administrative Patent Judge*.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1-20.
We have jurisdiction of this appeal under 35 U.S.C. § 6(b). We affirm.

STATEMENT OF CASE

The claimed invention is directed to a method of fabricating an electronics package comprising a die, a pin carrier, and an electronic component in the cavity of the pin carrier. The method comprises a step in which the pin carrier cavity is substantially filled with an encapsulant. The

dispute in patentability between the Examiner and the Appellant turns on the obviousness of this step. The Examiner relies on the following evidence of unpatentability:

Applicant Admitted Prior Art (AAPA) as described on page 3 of the Specification and shown in application Figs. 1-2

Wakashima US 2002/0020909 A1 Feb. 21, 2002

Claims 1-20, which are all the pending claims, stand rejected under 35 U.S.C. § 103(a) as obvious over AAPA in view of Wakashima (Answer 3). Because Appellant has not separately argued the patentability of any individual claims, the claims stand or fall together. *See* 37 C.F.R. § 41.37(c)(1)(vii). We select claim 1 as representative to decide all issues in this appeal. Claim 1 reads as follows:

1. A method of fabricating an electronics package, the method comprising:

securing a die to one side of an interposer, the interposer being a tape having a thickness less than 1 mm;

securing a pin carrier to an opposing side of the interposer, the pin carrier including a cavity positioned against the interposer opposite to the die;

securing an electronic component to the interposer such that the electronic component is positioned within the cavity in the pin carrier; and

substantially filling the cavity in the pin carrier with an encapsulant while not overflowing the cavity with the encapsulant such that the interposer is capable of withstanding a mechanical load generated by thermal elements and is incapable of withstanding the mechanical load without the encapsulant.

DISCUSSION

“Integrated circuits (ICs) have typically been assembled into electronic packages by physically and electrically coupling them to a substrate made of organic or ceramic material” (Spec. 1: 13-15). “A typical package includes an IC, such as a die, that is mounted on an interposer which functionally connects the die through a hierarchy of electrically conductive paths to the other elements, such as other ICs, that make up the electronic system” (Spec. 2: 3-6).

To address circuitry problems, such as loop induction, capacitors are typically attached to the underside of a thin interposer (Spec. 2: 18-25; Fig. 2). “[T]he thin interposer leads to another problem as the thin interposer is unable to handle the mechanical loads that are applied by the heat sinks which are typically used to cool the integrated circuit” (Spec. 2: 25-27). “The present invention provides a solution to thickness, weight, and/or rigidity limitations in an electronic package, and to loop induction problems that are associated with prior art electronic packages” (Spec. 4: 26-28). The cavity on the underside of the interposer is filled with “encapsulant [such as an epoxy] . . . [which] supports the thin interposer . . . in the area of the cavity . . . such that the package . . . is capable of withstanding the mechanical load that is applied to the package . . . by heat sinks and other thermal elements within the electronic assembly where the package . . . is located” (Spec. 5: 13-19).

The issue in this appeal is whether the Examiner erred in concluding that it would have been obvious to persons of ordinary skill in the art to have modified the method of producing the prior art electronic package (Spec.,

Fig. 2) by adding a step comprising filling the cavity on the underside of its interposer with an encapsulant.

Appellant admits that the electronics package is prior art (Spec. 3: 1-25; Answer 3). The admitted difference between the prior art and the electronics package made by the claimed method is that the latter comprises a manufacturing step in which its pin cavity is “substantially fill[ed]... with an encapsulant... while not overflowing the cavity... with the encapsulant... such that the interposer... is capable of withstanding a mechanical load generated by thermal elements and is incapable of withstanding the mechanical load without the encapsulant....” (Br. 6). Figs. 2 and 3 of the instant application, illustrating this admitted difference, are reproduced below:

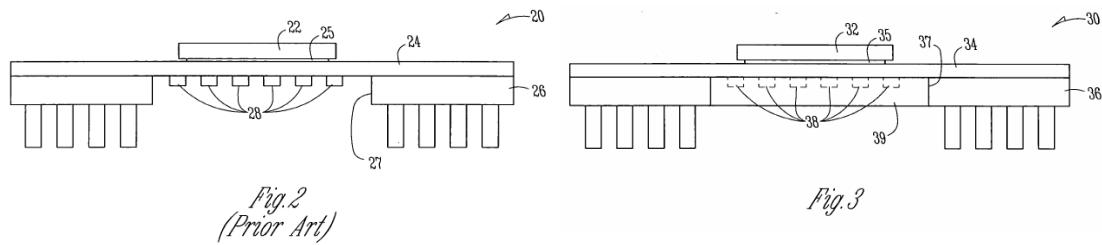


Fig. 2 shows the prior art electronics package; Fig. 3 shows an electronics package produced by a method of the claimed invention. The cavity is labeled “27”; the encapsulant is shown as “39.”

Wakashima is cited by the Examiner for its teaching of a semiconductor package comprising a gap located on the underside of a substrate 2 which is filled with a resin base 4 (Wakashima, Abstract; Answer 4). Figs. 2C and 2D of Wakashima are reproduced below.

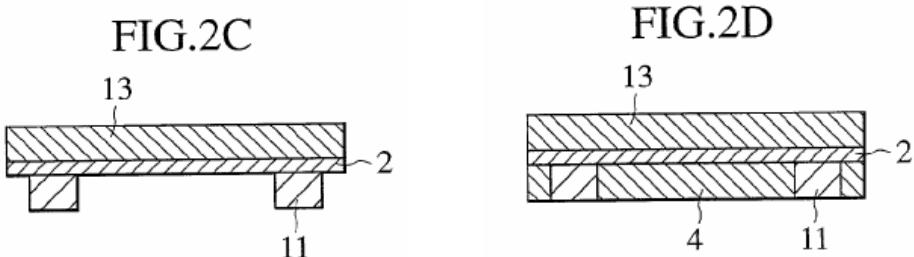


Fig. 2C shows the package prior to filling; Fig. 2D shows it after filling.

Wakashima teaches that “[b]y filling the gap with a resin, the mechanical strength of the substrate is guaranteed” (Wakashima, [0043]). The Examiner contends that Wakashima’s semiconductor package is “analogous” to the claimed electronics package (Answer 4). The Examiner concludes that it would have been obvious to one of ordinary skill in the art at the time the invention was made to have filled the prior art electronic package’s cavity with an encapsulant to strengthen the interposer as taught by Wakashima (Answer 4, 6).

Appellant contends that Wakashima does not describe “a cavity in a pin carrier as recited in the claims” nor “substantially filling the pin carrier with an encapsulant” (Br. 10; Reply Br. 1). Thus, Appellant asserts that the admitted prior art combined with Wakashima does not describe every element of the claimed invention (Br. 9-10).

In our opinion, too much emphasis has been placed by Appellant on whether Wakashima teaches “a cavity in a pin holder,” without addressing the Examiner’s reason for relying on Wakashima: for its teaching of a resin base to strengthen a thin interposer substrate.

Wakashima describes a semiconductor package with a chip on one side of a substrate and pillar interconnections on the other side of the substrate. We agree with the Examiner that this package is “analogous” to

an electronics package, where the substrate has a function similar to the interposer. A “gap” is formed on the substrate (2) underside when metal (1) is etched, leaving a hollow space surrounded by “pillar-like interconnections (11)” in the unetched regions (Wakashima, [0042]). The hollow is filled in with a resin base 4 to increase its mechanical strength (Wakashima, [0043]). “The thickness of the pillar-like interconnection 11 is 12 μm to 100 μm If the thickness of the interconnection 11 is less than 12 μm , the resin base 4 also becomes thin, and the mechanical strength of the substrate decreases. In addition, the insulating ability of the resin base 4 deteriorates” (Wakashima [0031]).

Thus, Wakashima teaches that etching the metal to produce a hollow region between pillar-like interconnections reduces the thickness of the substrate/metal in the etched region, decreasing its mechanical strength and insulating ability. Persons of skill in the art would have recognized this is the same defect that occurs in the prior art electronics package when the interposer is hollowed to accommodate the pin carrier.¹ Whether this region is characterized as a “cavity” or a “gap,” is not dispositive since in each case there is a hollow region having a thin ceiling (substrate or interposer) of reduced mechanical strength. Wakashima teaches filling it with a resin to “guarantee” its mechanical strength (Wakashima, [0043]). We agree with the Examiner that this constitutes a strong teaching that package strength can be increased by filling hollow spaces with resin, prompting the skilled worker to have modified the admitted prior art electronics package.

¹ It also appears that Appellant admits that the thin interposer of the prior art package was known to be a problem because of its reduced mechanical strength (Spec. 2: 25-27; 3: 20-25).

In attempting to distinguish the claimed invention from Wakashima, Appellant contends

. . . that AAPA and Wakashima et al. teach away from any type of combination. AAPA describes placing a pin carrier 26 onto an interposer 24. Wakashima et al. describes attaching solder balls 12 to interconnections 11 in a substrate (see, e.g., FIG. 1 and paragraph 35 of Wakashima et al). Applicant can not see how the substrate 10 and solder balls 12 of Wakashima et al. could be incorporated into the interposer/pin carrier/cavity/electronic component configuration of AAPA.

(Br. 14.)

We do not find this argument persuasive. As noted by the Examiner (Answer 9), the rejection does not depend on incorporating Wakashima's substrate and solder balls into the prior art package. "Wakashima is used only to show the obviousness of using resin material. This material, therefore, may be used in either a pin grid array or bump grid array" (Answer 9). Other than identifying a difference in the type of electronic connector, Appellant has not explained why this difference would have led the skilled worker to view the solution for strengthening a thin substrate of reduced mechanical strength in Wakashima's semiconductor package as inapplicable to an electronic package comprising pins – which are analogous in function.

Appellant also argues that "that the only teaching or suggestion as to 'securing an electronic component to the interposer such that the electronic component is positioned within the cavity in the pin carrier' in combination with 'substantially filling the cavity in the pin carrier with an encapsulant' is found in Applicant's disclosure" (Br. 11). *See also* Br. 14, 15. We are not convinced by this argument. Based on admissions in the instant

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Specification (Spec. 3), the Examiner concluded that the manufacturing process recited in claim 1 was known – except for the step of “substantially filling the cavity in the pin carrier with an encapsulant.” Appellant does not dispute that the claimed process steps, including securing an electronic component to a cavity within the pin carrier, were known. Wakashima describes filling a gap with resin at a thin region of a substrate in a semiconductor package in order to strengthen it. This description is relied upon by the Examiner as a *teaching or suggestion* to have modified the process for manufacturing the prior art electronic package. Thus, the Examiner has identified all elements of the claimed invention in the prior art and a reason to have modified it to arrive at the claimed invention.

For the foregoing reasons, we affirm the rejection of claim 1. Claims 2-19 fall with claim 1 because separate arguments for their patentability were not presented. Arguments not made are waived. *See* 37 C.F.R. § 41.37(c)(1)(vii).

TIME PERIOD

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv)(2006).

AFFIRMED

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