

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SOLID DATA SYSTEMS, INC.

Appeal 2007-2361
Reexamination Control 90/005,728 and 90/005,401¹
Patent 5,555,402
Technology Center 2100

Decided: November 27, 2007

Before JAMESON LEE, SALLY C. MEDLEY, and JAMES T. MOORE,
Administrative Patent Judges.

MEDLEY, *Administrative Patent Judge.*

DECISION ON APPEAL

A. Statement of the Case

This appeal under 35 U.S.C. §§ 134 and 306 is from a final rejection of claims 1-7, 20 and 21. We have jurisdiction under 35 U.S.C. § 6(b).

¹ Application for patent filed 16 May 2000. The reexamination proceedings were merged in accordance with 37 CFR 1.565(c) (09/005,401 and 90/005,728, 26 February 2001 Decision to merge).

C. Findings of fact

The record supports the following findings of fact as well as any other findings of fact set forth in this opinion by at least a preponderance of the evidence.

1. Claims 1-7, 20 and 21 are the subject of this appeal.

2. Independent claim 1, the sole independent claim, was amended during reexamination, and is as follows (amended language in bold italics):

1. A disk storage subsystem for storing data supplied by a disk controller and retrieving data needed by said disk controller, wherein said disk controller specifies a storage location by geometric address information, said disk storage subsystem comprising:

a volatile storage medium;

a parallel path;

a nonvolatile media;

a control circuit comprising a first port, a second port, a first control line and a second control line, wherein said first port is operatively coupled to said nonvolatile media, said second port is operatively coupled to said parallel path, said first control line is operatively coupled to said volatile storage medium and said second control line is operatively couplable to said disk controller;

wherein in a first mode of operation, in response to a first control signal from said disk controller, said control circuit stores ***over said parallel path*** data received from said disk controller at a location in said volatile storage medium corresponding to geometric address information;

in a second mode of operation, in response to a second control signal from said disk controller, said control circuit retrieves *over said parallel path* data from a location in said volatile storage medium corresponding to said geometric address information and provides said retrieved data to said disk controller; and

further wherein said control circuit can store parallel data received on said parallel path into said nonvolatile media and supply parallel data from said nonvolatile media on said parallel path.

3. SDS amended claim 1 by adding the above highlighted language and explained the amended claim 1 as follows:

... Fig. B (attached) in accordance with Claim 1 shows similarly the host disk controller which is the source of the data. But here the control circuit has two ports, P1 and P2, on its left side. Port P2 is connected by the horizontal bus to the volatile RAM memory and port P1 is connected by another bus to the non-volatile hard disk. As shown, in the first mode (Mode 1) in accordance with Claim 1, data is written from the host disk controller through the control circuit into the volatile memory. In the second mode (Mode 2), data is read out from the volatile memory to the control circuit, back to the host disk controller (Response to Final Rejection, 18 July 2001 at 5).

Appeal 2007-2361

Reexamination Control 90/005,728 and 90/005,401

4. A copy of the Fig. B sketch made by SDS that is referred to above is reproduced below (Response to Final Rejection, 18 July 2001 at 16 (attached)).

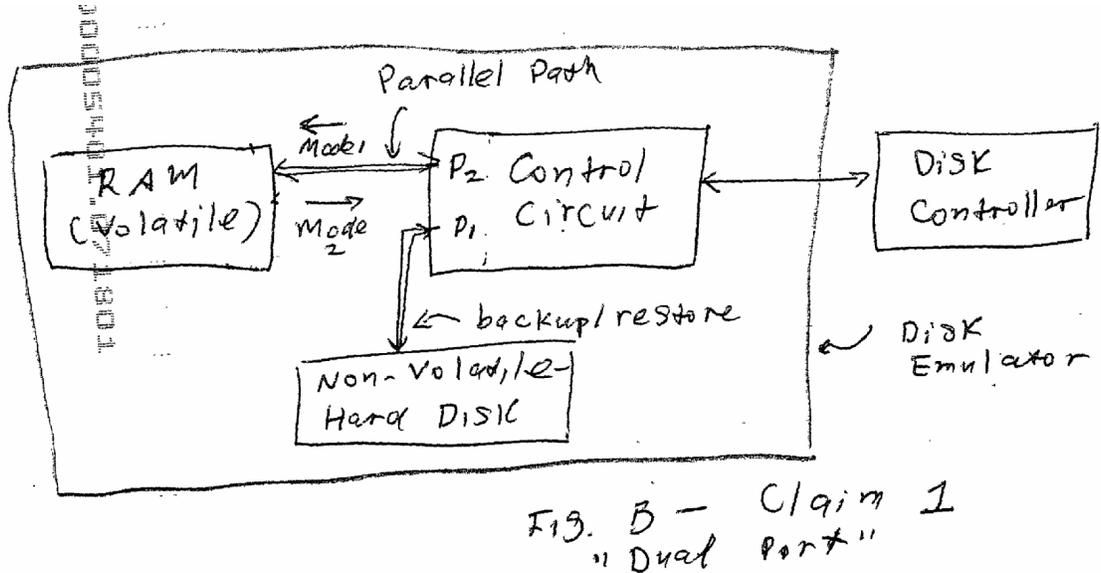


Fig. B depicts SDS' explanation of its amended claim 1.

5. The Examiner rejected claims 1-7, 20 and 21 under 35 U.S.C. 112, ¶ 2 on the basis that the added highlighted language from above renders the claim indefinite.

6. The Examiner found that claim 1 recites a single parallel path that has two distinct structural paths depending on the claimed mode of operation.

7. The Examiner found that the parallel path in the claimed first and second modes of operation reads on parallel path 113 and 112 (FIG. 2) and that the parallel path recited as operatively connected to the second port and claimed in the last wherein clause (the backup mode) reads on the SCSI data

Appeal 2007-2361

Reexamination Control 90/005,728 and 90/005,401

path 118 (FIG. 2 – SCSI DATA PATH) and that those are two distinct paths (Answer at 6).

8. The Examiner concluded that claim 1 is indefinite since the claim recites two separate and distinct buses (paths) in operation as one single bus (path), and that the claim is confusing since a single structurally claimed bus (path) should direct data over the same path and not to two different destinations (over two distinct paths) (Answer at 7).

9. SDS argues that the parallel path includes path 118, 102, data path 113, 112 to SOLID STATE MEMORY 104 (Appeal Br. 8³).

10. SDS argues that during the read/write mode (e.g., the claimed first and second modes of operation) data flows only over a portion of the parallel path – over parallel bus 112, 113 (Appeal Br. 7-8).

11. In its brief, SDS argues that:

It is clear (see patent FIG. 2) that the during the normal READ/WRITE mode (no backup), during writing the data is provided from SMD DISK CONTROLLER 107 over write data line 115 to the serializer/deserializer 102 and hence, via the parallel path 113, 112 to the SOLID STATE (volatile) MEMORY 104. During the backup phase, the data passes, for instance when data is to be backed up, from SOLID STATE MEMORY 104 through path 112, 113 through the serializer/deserializer 102, then via SCSI path 118 to the control circuit 100 and finally to the SCSI hard disk (non-volatile media) 101.

12. SDS characterizes the first mode of operation as the described

³ We refer to the 25 January 2006 Appeal Brief.

Appeal 2007-2361

Reexamination Control 90/005,728 and 90/005,401

write operation (FIG. 2 - storing data from disk controller 107 into volatile storage medium 104); the second mode of operation as the described read operation (FIG. 2 - reading data out of solid state memory 104 back to the disk controller 107); and the “further wherein” operation recited at the end of claim 1 as the backup mode (control circuit 100 backs up data stored in solid state memory 104 into SCSI hard disk 101) (Appeal Br. 5).

13. SDS argues that neither the specification nor claim 1 require that the entire data flow be over the same path – merely that at least a part of the “parallel path” be used for both (Appeal Br. 9 and Aug. 15, 2007 transcript 25:3-8).

14. SDS argued for the first time, in its reply brief, that the Examiner’s rejection of the claims 1-7, 20 and 21 under 35 U.S.C. 112, ¶ 2 is improper, since the rejection must be limited to “subject matter added or deleted in the re-examination proceeding” presumably in reference to 37 CFR 1.552(a) (Reply Br. 3, Aug. 15, 2007 transcript at 4:1-19).

15. SDS argues that the Examiner’s 112, ¶ 2 rejection applied to the subject matter of the originally patented claim 1 and is improper (Reply Br. 3).

16. During oral argument the following exchange took place:

MR. KLIVANS: All right. So the issue is, how does claim 1 read on figure 2 with regard to the parallel path? Now, there are several main elements here; the one, if you look in the center of this figure, there is a sold state memory block 104, that's what's referred to in the patent claims as a volatile storage medium because it doesn't retain the data for a long time. The

non-volatile storage medium is a skuzzy hard disk 101 in the lower left hand part of the figure, so it's important you -- those are the two elements that are actually storing data. Then you see on the right hand side there is a SND disk controller 107; that's the disk controller in the claim. So, what happens is in the operation of the device typically the data is going to be stored and read from the solid-state memory 104. And this happens, if you look at the figure, the data comes from the disk controller on the data line 114 and it goes into that serializer-deserializer 102, then it goes down to the error on the path 113 through the error correction circuit 103, and then on path 112 into the solid state memory 104. That's when you're writing data into the solid-state memory 104. Then when the data is read out of that, it's read on the reverse path from 104 through 112 to 103, 113 through the serializer, then back out to the SND disk controller.

JUDGE MOORE: All of which is conventional?

MR. KLIVANS: Yes, that's the normal reading and writing and when we talk about in the patent claim the first mode of operation, that's the writing of the data into that solid state memory. And then in the second mode is the reading of the data from the solid-state memory, which is backwards from the solid-state memory back out to the disk controller. That's the conventional reading and writing, like you said, Judge. The third part, and the last part of the claim, the last paragraph of the claim, is the backup mode, and that's when the data is transferred into and out of the hard disk 101 at the bottom left hand side of the figure. And that happens on the path 118, because what happens is, the data has to go from the solid state memory 104 back up on 112 to the error correction circuit and then up through 113 and then back down on path 118 through the control circuit back into the skuzzy hard disk. That's the backup mode. The backup mode is typically used when the tower has failed to the system and you want to read the data out of that solid state memory and save it on the hard disk.

Appeal 2007-2361

Reexamination Control 90/005,728 and 90/005,401

JUDGE MEDLEY: So parallel path then is 118, 113 and 112?

MR. KLIVANS: For that purpose, yes. Correct. Those are -- by parallel path we mean the path can carry a number of signals simultaneously, typically of course on a number of parallel lines or a buss. That's why it's called a parallel path. It's really a parallel data path.

D. Principles of Law

35 U.S.C. § 112, ¶ 2

A claim is indefinite if, when read in light of the Specification, it does not reasonably apprise those skilled in the art of the scope of the invention. *Amgen Inc. v. Hoechst Marion Roussel, Inc.*, 314 F.3d 1313, 1342 (Fed. Cir. 2003). Specifically, if the scope of the invention sought to be patented cannot be determined from the language of the claims, the Specification or the teachings of the prior art with a reasonable degree of certainty, a rejection of the claims under 35 U.S.C. § 112, second paragraph is appropriate. *In re Wiggins*, 488 F.2d 538, 541 (CCPA 1973).

E. Analysis

The 112, ¶ 2 rejection

SDS argued, for the first time in its reply, that the Examiner's rejection of the claims under 35 U.S.C. 112, ¶ 2 was improper, apparently based on 37 CFR 1.552(a) (FF⁴ 14).

To quote the Seventh Circuit, SDS' argument in its Reply regarding

⁴ FF denotes finding of fact.

Appeal 2007-2361

Reexamination Control 90/005,728 and 90/005,401

the propriety of the Examiner's rejection comes "too late." *De Silva v. DiLeonardi*, 181 F.3d 865, 867 (7th Cir. 1999). One should know that an argument presented for the first time in a reply brief generally will not be considered. *See, e.g., Carbino v. West*, 168 F.3d 32, 34 (Fed. Cir. 1999); *Kaufman Co. v. Lantech, Inc.*, 807 F.2d 970, 974, (Fed. Cir. 1986); *Ernst Haas Studio, Inc. v. Palm Press, Inc.*, 164 F.3d 110, 111-12 (2d Cir. 1999); *United States v. Oakley*, 744 F.2d 1553, 1556 (11th Cir. 1984); *General Carbon Co. v. Occupational Safety & Health Review Commission*, 854 F.2d 1329, 1330 (D.C. Cir. 1988); and *Asociacion de Compositores y Editores de Musica Latinoamericana v. Copyright Royalty Tribunal*, 809 F.2d 926 (D.C. Cir. 1987).

SDS should have addressed the alleged impropriety of the Examiner's final rejection in their Appeal Brief.

In any event, SDS has failed to sufficiently demonstrate that the Examiner's rejection was improper. 37 CFR 1.552(a) states that:

Claims in an ex parte reexamination proceeding will be examined on the basis of patents or printed publications and, with respect to subject matter added or deleted in the reexamination proceeding, on the basis of the requirements of 35 U.S.C. 112.

According to SDS, the Examiner's 35 U.S.C. 112, ¶ 2 rejection based on the added limitation "over said parallel path" is improper because the language "parallel path" was in original claim 1 and is therefore not "subject matter added." Prior to adding the amended language (FF 2 - highlighted

Appeal 2007-2361

Reexamination Control 90/005,728 and 90/005,401

language), there was no limitation as to how the data traveled during the first and second modes of operation – over the parallel path. The added limitation changes the scope of the claim and qualifies as “added subject matter” within the meaning of the rule. The standard is not whether the same words appear elsewhere in the original claim. Therefore, the rejection is proper.

Claim 1 recites during a first mode of operation and in response to a first control signal from the disk controller “said control circuit stores over said parallel path data received from said disk controller at a location in said volatile storage medium corresponding to geometric address information.” Claim 1 also recites during a second mode of operation and in response to a second control signal from the disk controller “said control circuit retrieves over said parallel path data from a location in said volatile storage medium corresponding to geometric address information and provides said retrieved data to said disk controller.”

According to the Examiner, the “over said parallel path” limitation recited in connection with the first and second modes of operation renders the claim indefinite. Specifically, the Examiner found that the “parallel path” associated with the two modes of operation is structurally different than the “parallel path” recited elsewhere in claim 1 and therefore claim 1 should be interpreted as reciting two structurally distinct parallel paths (FFs 5-8) .

The plain language of claim 1 recites only one parallel path, not two.

Appeal 2007-2361

Reexamination Control 90/005,728 and 90/005,401

The Examiner is apparently importing limitations from the specification into claim 1 in support of the argument that the claim should be interpreted as reciting two structurally different parallel paths (FFs 7-8). However, the name of the game is the claim. *In re Hiniker Co.*, 150 F.3d 1362, 1369 (Fed. Cir. 1998). Structural elements from the specification should generally never be imported into a claim⁵.

Nonetheless, we agree with the Examiner that the mode of operation limitations with the “over said parallel path” render claim 1 indefinite for the following reasons.

There are two plausible interpretations for the “mode of operation” limitations. The first way to interpret the mode of operation limitations results in the control circuit being operatively coupled in between the volatile storage medium and the disk controller, where the parallel path operatively connects the control circuit and the volatile storage medium. In the first mode of operation, the control circuit stores data (over the parallel path) received from the disk controller at a location in the volatile storage medium. In the second mode of operation, the control circuit retrieves data (over the parallel path) from the volatile storage medium and provides the data to the disk controller. If we were to draw a picture, the picture would show the control circuit in between the volatile storage medium and the disk

⁵ A claim that is inconsistent with the specification may properly be rejected under 35 U.S.C. 112, ¶ 1 based on the written description requirement. Here, however, the Examiner made no such rejection.

Appeal 2007-2361

Reexamination Control 90/005,728 and 90/005,401

controller, where the parallel path operatively couples the control circuit to the volatile storage medium. The picture would resemble SDS' Fig. B relied on by SDS to explain its amended claim 1 (FF 4).

The above interpretation is consistent with SDS' explanation of amended claim 1 and its Fig. B presented during prosecution (FFs 3 and 4), where SDS explained that:

[In] the first mode (Mode 1) in accordance with Claim 1, data is written from the host disk controller through the control circuit into the volatile memory. In the second mode (Mode 2), data is read out from the volatile memory to the control circuit, back to the host disk controller (FF 3).

The second way to interpret the limitation results in the parallel path being coupled in between the volatile storage medium and the disk controller. In the first mode of operation, the control circuit stores, by way of control signals for example, data from the disk controller over the parallel path to a location in the volatile storage medium. In the second mode of operation, the control circuit retrieves, by way of control signals for example, data from the volatile storage medium over the parallel path to the disk controller. If we were to draw a picture, the picture would show a parallel path coupled between the disk controller and the volatile storage medium. The control circuit merely orchestrates the storing of data by sending a control signal⁶. This interpretation is consistent with the

⁶ This is described for example at col. 13, line 33 to col. 14, line 29, with reference to Fig. 2. For example, in write mode, we understand that disk

Appeal 2007-2361

Reexamination Control 90/005,728 and 90/005,401

arguments most recently advanced by SDS and is apparently the interpretation currently urged by SDS (FFs 9-12 and 16).⁷ For example, SDS argues in their brief that:

It is clear (see patent FIG. 2) that the during the normal READ/WRITE mode (no backup), during writing the data is provided from SMD DISK CONTROLLER 107 over write data line 115 to the serializer/deserializer 102 and hence, via the parallel path 113, 112 to the SOLID STATE (volatile) MEMORY 104 (FF 11).

So interpreted, the claim reads directly on Figure 2 of the involved patent.

The two different interpretations arise due to confusing grammatical sentence structure. Either interpretation is plausible. Both interpretations have been presented and apparently accepted by SDS as plausible interpretations. We do not take the view that the claim is broad enough to cover both interpretations, because clearly it can not. The two different interpretations result in two different structural arrangements. The patent owner has argued them both and we have no clear reason to favor one over the other. One is more in line with the literal language of the claim but does

controller 107 sends a write signal 120 to control circuit 100. Control circuit 100 sends a write signal to solid state memory 104. Upon receiving commands, data from disk controller 107 passes over write data line 115, which is deserialized by serializer/deserializer circuit 102 into parallel data. The parallel data passes over path 113, 112 and is stored in solid state memory 104.

⁷ SDS apparently no longer urges the first interpretation, but rather the second one.

Appeal 2007-2361

Reexamination Control 90/005,728 and 90/005,401

not read on a disclosed preferred embodiment. The other is reasonable and reads well on Figure 2. The claim is so confusing that even the patent owner has flip-flopped on the proper reading without adequate accounting. For all of these reasons, the scope of the invention sought to be patented cannot be determined from the language of claim 1 with a reasonable degree of certainty and we therefore sustain the Examiner's rejection of claims 1-7, 20 and 21 under 35 U.S.C. § 112, ¶2 as being indefinite.

Because the metes and bounds of the claims are speculative, we do not reach the prior art rejections. *In re Steele*, 305 F.2d 859, 863 (CCPA 1962).

F. Decision

Upon consideration of the record, and for the reasons given, the Examiner's rejection of claims 1-7, 20 and 21 under 35 U.S.C. § 112, ¶2 as being indefinite is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED

VW

Appeal 2007-2361
Reexamination Control 90/005,728 and 90/005,401

cc (via First Class Mail):

MORRISON & FOERSTER LLP
755 PAGE MILL RD
PALO ALTO CA 94304-1018