

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte WILBUR H. HIGHLEYMAN, PAUL J. HOLENSTEIN,
and BRUCE D. HOLENSTEIN

Appeal 2007-3099
Application 10/367,675
Technology Center 2100

Decided: February 6, 2008

Before JAMES D. THOMAS, LANCE LEONARD BARRY,
and JAY P. LUCAS, *Administrative Patent Judges*.

THOMAS, *Administrative Patent Judge*.

DECISION ON APPEAL

This appeal involves claims 1 through 12. We have jurisdiction under 35 U.S.C. §§ 6(b) and 134(a). The oral hearing set for January 23, 2008, was waived in a facsimile communication received on December 26, 2007.

As best representative of the disclosed and claimed invention, independent claim 1 is reproduced below:

1. A method of assigning processors in a multiprocessor environment to a plurality of processes that are executed in the multiprocessor environment, each process having a process pair defined by a primary process that executes on a first processor and a backup process that executes on a second processor, the processors being in communication with one another via a communication network, the method comprising:
 - (a) organizing the plurality of processors into predefined processor pairs, wherein each processor is assigned to only one processor pair; and
 - (b) assigning every process pair to one of the processor pairs.

The following references are relied on by the Examiner:

Horst	US 6,496,940 B1	Dec. 17, 2002
		(Filed date Jun. 7, 1995)
de Azevedo	US 6,665,811 B1	Dec. 16, 2003
		(Filed date Aug. 24, 2000)

Rather than repeat the positions of the Appellants and the Examiner, reference is made to the Brief and Reply Brief for Appellants' positions, and to the Answer for the Examiner's positions.

OPINION

For the reasons set forth by the Examiner in the Answer, as embellished upon here, we sustain the rejection under 35 U.S.C. § 103 of claims 1 through 12 on appeal. The Brief and Reply Brief emphasize only certain common features of independent claims 1, 4, and 7 on appeal (of which claim 1 is representative) and present no arguments as to any dependent claims on appeal.

PRINCIPLES OF LAW

Appellants have the burden on appeal to the Board to demonstrate error in the Examiner's position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006) ("On appeal to the Board, an applicant can overcome a rejection [under § 103] by showing insufficient evidence of *prima facie* obviousness or by rebutting the *prima facie* case with evidence of secondary indicia of nonobviousness.") (quoting *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998)).

The *claims* measure the invention. *See SRI Int'l v. Matsushita Elec. Corp.*, 775 F.2d 1107, 1121 (Fed. Cir. 1985) (en banc). "[T]he PTO gives claims their 'broadest reasonable interpretation.'" *In re Bigio*, 381 F.3d 1320, 1324 (Fed. Cir. 2004) (quoting *In re Hyatt*, 211 F.3d 1367, 1372 (Fed. Cir. 2000)). "Moreover, limitations are not to be read into the claims from the specification." *In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993) (citing *In re Zletz*, 893 F.2d 319, 321 (Fed. Cir. 1989)). Our reviewing court has repeatedly warned against confining the claims to specific embodiments described in the specification. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1323 (Fed. Cir. 2005) (en banc). During prosecution before the USPTO, claims are to be given their broadest reasonable interpretation, and the scope of a claim cannot be narrowed by reading disclosed limitations into the claim. *See In re Morris*, 127 F.3d 1048, 1053-54 (Fed. Cir. 1997); *In re Zletz*, 893 F.2d 319, 321 (Fed. Cir. 1989); *In re Prater*, 415 F.2d 1393, 1404-05 (CCPA 1969).

"[T]he words of a claim 'are generally given their ordinary and customary meaning.'" *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (internal citations omitted). "[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." *Phillips v. AWH Corp.*, 415 F.3d at 1313 (Fed. Cir. 2005) (en banc).

In the absence of separate arguments with respect to claims subject to the same rejection, those claims stand or fall with the claim for which an argument was made. *See In re Young*, 927 F.2d 588, 590 (Fed. Cir. 1991). *See also* 37 C.F.R. § 41.37(c)(1)(vii)(2004).

As to the other recited elements of representative independent claim 1, Appellants provide no arguments to us to dispute that the Examiner has correctly shown where all these claimed elements appear in the prior art. Thus, we deem those arguments waived. *See* 37 C.F.R. § 41.37(c)(1)(vii) (2004).

ANALYSIS

Appellants have not shown that the Examiner has erred in finding claims 1 through 12 unpatentable over the teachings and suggestions of Horst and de Azevedo within 35 U.S.C. § 103.

The Examiner has repeatedly pointed out in the Answer the significant portions of both references that are dispositive of the issues presented in this appeal. Appellants' positions with respect to Horst beginning at page 7 of

the principal Brief recognize that process pairing was admitted by them to be in the prior art of this reference. We totally disagree with Appellants' view that this reference does not teach or suggest that two processors may be associated with any type of processor pair. Appellants' approach admits that Horst teaches either in the admitted prior art of this reference or in its own teachings the features of "assigning every process pair to one of the processor pairs" in clause B of representative independent claim 1 on appeal and its related reliance upon clause A of that claim that requires each processor to be assigned to only one processor pair. The artisan would well understand that at least the duplex-mode dual CPU pairing discussed generally at column 6 of Horst also processes dual, paired processes since its reference plainly teaches that separate, paired process instruction streams are processed simultaneously and in lock-step, synchronous fashion by paired CPUs.

We are unpersuaded by an alleged distinction made between what Horst regards as the admitted prior art approaches at columns 1 through 4 and the contribution beginning in the Summary of the Invention provided by Horst himself. The significant discussion at columns 1 and 2 by Horst regarding the fault tolerant machines provided by Tandem Computers emphasizes at column 2 in the prior art that plural processes are copied in separate processors in the form of duplicate copies of the same operating system; the latter portions of column 2 emphasize that this technique applies to application software as well. The so-called "I'm Alive" teachings in the prior art of Horst are also discussed beginning at column 1 in de Azevedo. Contrary to the views taken by Appellants in the Brief and Reply

Brief, Horst does teach a correlation between process pairs and their interrelationship with processor pairs as broadly recited in representative independent claim 1 on appeal.

Moreover, de Azevedo contains complementary teachings which are cumulative to what is already taught in Horst as to the subject matter of representative independent claim 1 on appeal. Besides the “I’m Alive” correlation noted earlier in this appeal, de Azevedo also relates to fault tolerant distributed or clustered multiprocessor systems. The discussion at the middle of column 1 relied upon by the Examiner confirms independently what Horst already teaches that primary processes and backup processes with plural processors in a paired fashion are known to exist in the art.

Independent claim 4 may arguably be considered to be broader than independent claim 1 because it does not necessarily require a “backup” process but merely more broadly an additional “active” process which is inclusive of a backup process. This is well known in the art as evidenced by both references relied upon by the Examiner since the more specific backup feature of claim 1 is clearly met. Correspondingly, the recitations in claim 7 are also taught by the applied prior art. Because of the significant use of the alternative “or,” more than two (a pair) of processors and/or processes are not required by this claim, contrary to the position evidently taken by Appellants in the Brief and Reply Brief. No distinctions are seen to exist with the use of the word “group” by itself over the paired approaches among the two references relied upon by the Examiner. A pair may be considered a “group.” Moreover, the Examiner has already indicated in the Answer that the discussion at the middle of column 3 of Horst contemplates

triple-modular-redundancy processors and processes which are also taught at the bottom of column 1 of this reference.

Lastly, it deserves to be said here that the alleged deficiency in the paragraph bridging columns 3 and 4 of Horst between the pure hardware redundancy and fault tolerant approaches of the prior art versus separate pure software redundancy fault tolerant approaches also of the prior art are solved according to Horst's teachings unifying them both beginning in the Summary of the Invention describing his contributions in the art.

In view of the foregoing, the decision of the Examiner rejecting all claims on appeal under 35 U.S.C. § 103 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a). *See* 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

pgc

PANITCH SCHWARZE BELISARIO & NADEL LLP
ONE COMMERCE SQUARE
2005 MARKET STREET, SUITE 2200
PHILADELPHIA PA 19103