

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte TORU IWAGAMI and MAMORU SEO

Appeal 2007-3229
Application 10/898,364¹
Technology Center 2800

Decided: January 23, 2008

Before JAMESON LEE, RICHARD TORCZON and SALLY C. MEDLEY,
Administrative Patent Judges.

MEDLEY, *Administrative Patent Judge.*

DECISION ON APPEAL

¹ Application for patent filed 26 July 2004. The real party in interest is MITSUBISHI DENKI KABUSHIKI KAISHA.

A. Statement of the Case

This is an appeal under 35 U.S.C. § 134 from the Examiner's Final Rejection of claims 1 and 10². We have jurisdiction under 35 U.S.C. § 6(b). We reverse and enter a new ground of rejection.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Ki	6,172,466	Jan. 9, 2001
Satoh	2002/0195682	Dec. 26, 2002
Ribarich	2004/0227471	Nov. 18, 2004

Claim 1 stands rejected as being unpatentable under 35 U.S.C. § 103(a) over Ribarich in view of Ki.

Claim 10 stands rejected as being unpatentable under 35 U.S.C. § 103(a) over Ribarich in view of Ki and further in view of Satoh.

BACKGROUND

The invention relates to an inverter circuit that includes first **3** and second **4** insulated gate bipolar transistors (IGBTs) connected in series between a power supply potential (**V_{cc}**) and a ground potential (**GND**), and a high voltage drive circuit (**HVIC**) **1** and a low voltage drive circuit (**LVIC**) **2** for respectively controlling actuation of the IGBTs **3**, **4**. The inverter circuit further includes a capacitor **5**, and a diode **6**. The capacitor **5** is connected between a terminal (**VS**) and **GND**. The diode **6** has a series connection to the capacitor **5** between the terminal **VS** and **GND**, with such a polarity that a forward current flows from **GND** to the terminal **VS**. A resistor **7** is connected in parallel to the capacitor **5** (**fig. 1**). Alternatively or

² Claims 2-9 have been withdrawn from consideration in the Office Action mailed 19 Jan. 2006.

additionally, a resistor **8** is connected in parallel to the diode **6** (**fig. 3**).
(Abstract, Spec. pp. 5-7).

B. Issues

The first issue before us is whether Applicants have shown that the Examiner erred in determining that claim 1 is unpatentable under 35 U.S.C. § 103(a) over Ribarich in view of Ki?

For the reasons that follow, Applicants have shown that the Examiner erred in determining that claim 1 is unpatentable under 35 U.S.C. § 103(a) over Ribarich in view of Ki.

The second issue before us is whether Applicants have shown that the Examiner erred in determining that claim 10 is unpatentable under 35 U.S.C. § 103(a) over Ribarich in view of Ki and further in view of Satoh?

For the reasons that follow, Applicants have shown that the Examiner erred in determining that claim 10 is unpatentable under 35 U.S.C. § 103(a) over Ribarich in view of Ki and further in view of Satoh.

C. Findings of Fact (“FF”)

The record supports the following finding of facts as well as any other findings of fact set forth in this opinion by at least a preponderance of the evidence.

1. Applicants’ claims 1 and 10 are the subject of this appeal.
2. Claim 1 is in independent form.
3. Claim 10 is dependent on claim 1.
4. Claim 1 is as follows:

An inverter circuit, comprising:
a high-voltage switching element and a low-voltage switching element connected in series between a power supply potential and a

GND potential; a high-voltage drive circuit having a terminal-
connected to a current emission terminal of said high-voltage
switching element to supply a reference potential to a high-potential
inner circuit in the high-voltage drive circuit, said terminal of said
high-voltage drive circuit being referred to as a terminal VS; and a
surge voltage suppressing circuit connected between said terminal VS
and said GND potential for suppressing a surge voltage generated
when the high-voltage switching element is turned off, the circuit
including

a capacitor;

a diode having a series connection to said capacitor with
such a polarity that a forward current flows from said GND
potential to said terminal VS; and

a resistor connected in parallel to one of said diode and
capacitor.

5. Claim 10 is as follows:

The inverter circuit according to claim 1, further comprising another
resistor connected in parallel to the other one of said diode and
capacitor.

6. The Examiner found that Ribarich describes an inverter circuit
comprising high-voltage **M1** and low-voltage switching elements **M2**
connected in series between power supply **1** and ground **3**, a high voltage
drive circuit **100** having a terminal **VS** connected to a current emission
terminal of said high voltage switching element (source/drain of the high
voltage switching element) while supplying a reference potential of high
potential inner circuit, and surge voltage suppressing circuit comprising a
capacitor **CSNUB** and diode **D1** (Final Rejection 2 and Ans. 3; Ribarich **fig.**
2).

7. The Examiner found that Ki describes a parallel connection of a
resistor and a capacitor connected to the output of an operational amplifier
(OP AMP) (Final Rejection 2 and Ans. 3; Ki fig. 4).

8. The Examiner found that it is known in the electronics art that parallel connection of a resistor and capacitor provides a filtering function for example, for filtering out unwanted noise or surge embedded in a signal (Final Rejection 2 and Ans. 3).

9. The Examiner concluded that it would have been obvious to one with ordinary skill in the art at the time the invention was made to include a resistor in parallel with Ribarich's capacitor for the purpose of filtering the output signal thus preventing an erroneous operation (Final Rejection 2 and Ans. 3-4).

10. The Examiner alternatively found that it is known in the electronic art that a filter circuit is used to filter out an unwanted noise or spike or surge embedded in the intended signal (Ans. 4-5).

11. The Examiner alternatively found that including a resistor in parallel to the capacitor of Ribarich would further enhance the suppressing function of Ribarich's surge voltage suppression circuit thus preventing an erroneous operation (Ans. 4-5).

12. The Examiner found that Satoh describes that by connecting a resistor in parallel with a diode, the variation in a resistive component of an LCR circuit formed by the diode will be suppressed (Final Rejection 3 and Ans. 4).

13. The Examiner concluded that it would have been obvious to person skilled in the art at the time the invention was made to include another resistor coupled in parallel with the Ribarich's diode for the purpose of suppressing the variation in a resistive component of an LCR circuit formed by the diode, thus preventing erroneous operation (Final Rejection 3 and Ans. 4).

D. Principles of Law

“Section 103 forbids issuance of a patent when ‘the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.’” *KSR Int’l Co. v. Teleflex Inc.*, 127 S.Ct. 1727, 1734 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, (3) the level of skill in the art. *Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966). *See also KSR*, 127 S.Ct. at 1734 (“While the sequence of these questions might be reordered in any particular case, the [*Graham*] factors continue to define the inquiry that controls.”) The Court in *Graham* further noted that evidence of secondary considerations, such as commercial success, long felt but unsolved needs, failure of others, etc., “might be utilized to give light to the circumstances surrounding the origin of the subject matter sought to be patented.” *Graham*, 383 U.S. at 18.

In *KSR*, the Supreme Court rejected the rigid application of the “teaching suggestion or motivation” (TSM) test, instead favoring the “expansive and flexible approach” used by the Court. 127 S.Ct. at 1739.

Despite the enactment of Section 103 and the *Graham* analysis there still remains “the need for caution in granting a patent based on the combination of elements found in the prior art.” *Id.*

Based on its precedent, the Court reaffirmed the principle that “[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results.” *Id.*

The Court's opinions in *United States v. Adams*, 383 U.S. 39 (1966), *Anderson's Black Rock Inc. v. Pavement Salvage Co.*, 396 U.S. 57 (1969) and *Sakraida v. Ag. Pro, Inc.*, 425 U.S. 273 (1976) are instructive when the question of whether an application claiming the combination of elements of prior art is obvious. *Id.* at 1740. In *Adams*, “[t]he Court recognized that when a patent claims a structure already known in the prior art that is altered by the mere substitution of one element for another known in the field, the combination must do more than yield a predictable result.” *Id.* at 1740 (citation omitted) (The Court ultimately found unexpected results resulting from prior art warnings to be dispositive of nonobviousness). In *Anderson's Black Rock*, the Court concluded that the claimed invention combining two pre-existing elements (radiant-heat burner and paving machine) ‘did not create some sort of new synergy’; each element functioned as expected. *Id.* at 1740. “The two in combination did no more that they would in separate, sequential operation”. *Id.* at 1740 (citations omitted). In *Sakraida*, “the Court derived from its precedents the conclusion that when [the claimed invention] ‘simply arranges old elements with each performing the same function it had been known to perform’ and yields no more than one would expect from such an arrangement, the combination is obvious.” *Id.* at 1740 (citations omitted).

When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, § 103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. [A] court must

ask whether the improvement is more than the predictable use of prior art elements according to their established functions.

Id. at 1740.

The Court further instructed that “the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim” and “inferences and creative steps that a person of ordinary skill in the art would employ” can be taken into account. *Id.* at 1741.

E. Analysis

Claim 1

Applicants apparently do not dispute the Examiner’s findings with respect to Ribarich. Rather, Applicants argue that the combination of Ribarich and Ki does not teach the claimed surge voltage suppressing circuit (App. Br. 5). Applicants admit that Ki appears to describe an RC (resistor-capacitor) filter but contend that Ki does not teach a resistor connected in parallel to a capacitor specifically in a surge voltage suppressing circuit that includes a diode in series with the capacitor (App. Br. 6). Applicants more particularly argue that the Examiner has not satisfied the burden of explaining why one with ordinary skill in the art would have realistically been motivated to make the proposed combination (App. Br. 6).

The Examiner determined that it was known at the time of the invention that a resistor and a capacitor in parallel provides a filtering function and that the connection of a resistor in parallel with a capacitor would have been obvious for filtering an output signal (FF 8-9).

Applicants acknowledge that a capacitor has a filtering function in general and that a resistor may be connected in parallel to the capacitor for

adjusting the time constant of a filter (App. Br. 6 and Reply Br. 4).

Applicants argue, however, that there is no prior art teaching that would have led a person with ordinary skill in the art to adjust a filter time constant for the purpose of suppressing a surge voltage (App. Br. 6). Applicants argue that filtering an output signal to prevent an erroneous operation as alleged by the Examiner would not have been a basis for one with ordinary skill in the art to connect a resistor in parallel with a capacitor to suppress a surge voltage (App. Br. 6-7). Applicants conclude that one skilled in the art would not have been motivated to connect Ki's resistor for adjusting the time constant of a filter in parallel to Ribarich's capacitor **CSNUB**.

In response, the Examiner argues that the quality of a filter depends directly on its time constant and that adjusting the time constant will modify the shape of the bandwidth (Ans. 5). The Examiner found that one skilled in the art would have known to adjust the time constant to minimize noise spike (Ans. 5). The Examiner also found that it is known in the electronic art that a filter circuit is used to filter out an unwanted noise, spike or surge embedded in a signal (FF 10). The Examiner alternatively found that including a resistor in parallel to the capacitor of Ribarich would further enhance the suppressing function of Ribarich's surge voltage suppression circuit thus preventing an erroneous operation (FF 11 and Ans. 4-5).

In response, Applicants assert that neither Ribarich nor Ki disclose nor suggest that the resistor of Ki enhances "the suppressing function of Ribarich's surge voltage suppressing circuit thus preventing an erroneous operation" (Reply Br. 4). Applicants argue that using a capacitor for suppressing a surge voltage does not require adjusting the time constant (Reply Br. 4). Applicants contend that it is not necessary to include a

resistor in parallel with a capacitor to suppress a surge voltage because, like a virtual short circuit, the resistor would be bypassed by the capacitor when it conducts the surge (Reply Br. 4).

While the Examiner has articulated a reason for the general desirability of filtering an output signal, we agree with Applicants that one with ordinary skill in the art would not have added a resistor in parallel with the Ribarich capacitor (**CSNUB**) for the purpose of “filtering” a voltage surge as suggested by the Examiner. A resistor so connected would not serve any further purpose for suppressing a surge during an over voltage event as alleged by the Examiner. For all these reasons, Applicants have sufficiently shown that the Examiner erred in determining that it would have been obvious to one with ordinary skill in the art to add a resistor in parallel to the capacitor or diode of Ribarich. Accordingly, Applicants have sufficiently shown error in the Examiner’s determination that claim 1 is unpatentable under 35 U.S.C. § 103(a) over the prior art.

Claim 10

Since the Examiner has applied the Ribarich and Ki references to the rejection of claim 10 in the same manner as claim 1, and because claim 10 includes all the limitations of claim 1, we find for the same reasons as explained above that Applicants have sufficiently shown error in the Examiner’s determination that claim 10 is unpatentable under 35 U.S.C. § 103(a) over the prior art.

New Ground of Rejection

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ribarich in view of Billings (6,107,751).

Ribarich describes an inverter circuit comprising high-voltage **M1** and low-voltage switching elements **M2** connected in series between power supply **1** and ground **3**, a high voltage drive circuit **100** having a terminal **VS** connected to a current emission terminal of said high voltage switching element (source/drain of the high voltage switching element) while supplying a reference potential to a high potential inner circuit, a surge voltage suppressing circuit **CSNUB**, **D1** connected between terminal **VS** and **GND** potential **3** the voltage suppressing circuit includes a capacitor **CSNUB** and a diode **D1** having a series connection to the capacitor **CSNUB** with such a polarity that a forward current flows from the **GND** potential to the **VS** terminal (**fig. 2**). Although Ribarich fails to describe a resistor connected in parallel to either the diode or the capacitor, attention is directed to Billings which describes a surge voltage suppressing circuit **230** (snubber circuit) that includes a diode **220** having a series connection to a capacitor **222** and a resistor **224** connected in parallel to the capacitor **222** (**fig. 3**).

Billings teaches that the resistor discharges the accumulation of energy across the capacitor (col. 8, ll. 63-67). It would have been obvious to one with ordinary skill in the art at the time the invention was made to modify the voltage suppressing circuit of Ribarich to include a resistor in parallel to the capacitor as described by Billings in order to discharge the accumulation of energy across the capacitor.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ribarich in view of Billings (6,107,751) as applied to claim 1 above and further in view of Yamanaka (6,226,192). Ribarich and Billings are as explained above. Although Ribarich and Billings fail to describe a resistor connected in parallel to the diode, attention is directed to Yamanaka which describes a similar voltage suppressing circuit **28** (snubber circuit) including a resistor **27** connected in parallel with a diode **25** that is connected in series with a capacitor **26** (**figs. 3, 4**) for the purpose of discharging the energy stored in the capacitor **26** when the capacitor **26** is not in a charging state (col. 5, l. 66-col. 6, l. 27). It would have been obvious to one with ordinary skill in the art at the time the invention was made to modify the voltage suppressing circuit of Ribarich as modified by Billings to include a resistor in parallel with the diode for the purpose of discharging the energy stored in the capacitor when the capacitor is not in a charging state.

The Ribarich device as modified by Billings and Yamanaka results in an arrangement of old elements “with each performing the same function it had been known to perform’ and yields no more than one would expect from

such an arrangement.”³ With this being the case, “the combination is obvious.”⁴

In the alternative, a rejection of claim 1 as unpatentable over Ribarich in view of Yamanaka (6,226,192) and a rejection of claim 10 as unpatentable over Ribarich in view of Yamanaka and further in view of Billings could be made based on the same findings.

Decision

Upon consideration of the record, and for the reasons given, the Examiner’s rejection of claim 1 as unpatentable under 35 U.S.C. § 103(a) over Ribarich in view of Ki is reversed.

Upon consideration of the record, and for the reasons given, the Examiner’s rejection of claim 10 as unpatentable under 35 U.S.C. § 103(a) over Ribarich in view of Ki and further in view of Satoh is reversed.

This decision contains a new ground of rejection pursuant to 37 C.F.R. § 41.50(b) (effective September 13, 2004, 69 Fed. Reg. 49960 (August 12, 2004), 1286 Off. Gaz. Pat. Office 21 (September 7, 2004)). 37 C.F.R. § 41.50(b) provides “[a] new ground of rejection pursuant to this paragraph shall not be considered final for judicial review.”

³ *KSR Int’l Co. v. Teleflex Inc.*, 127 S.Ct. 1727, 1740 (2007).

⁴ *Id.*

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37 CFR § 41.50(b) also provides that the appellant, WITHIN TWO MONTHS FROM THE DATE OF THE DECISION, must exercise one of the following two options with respect to the new ground of rejection to avoid termination of the appeal as to the rejected claims:

(1) *Reopen prosecution*. Submit an appropriate amendment of the claims so rejected or new evidence relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the proceeding will be remanded to the examiner. . . .

(2) *Request rehearing*. Request that the proceeding be reheard under § 41.52 by the Board upon the same record. . . .

REVERSED

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