

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MANOHAR K. PRABHU

Appeal 2007-3435
Application 09/952,994
Technology Center 2100

Decided: April 10, 2008

Before JAMES D. THOMAS, LANCE LEONARD BARRY, and
CAROLYN D. THOMAS, *Administrative Patent Judges*.

BARRY, *Administrative Patent Judge*.

DECISION ON APPEAL

I. STATEMENT OF THE CASE

A Patent Examiner rejected claims 1-19 and 41-82. The Appellant appeals therefrom under 35 U.S.C. § 134(a). We have jurisdiction under 35 U.S.C. § 6(b).

A. INVENTION

The invention at issue on appeal is a preemptive write back controller. Upon a hit to a write back cache during a processor's write operation, only the entry in the cache is written to and updated; the content of the main memory remains unaltered. The "dirty" entry to the cache is written back to main memory later to "clean" the cache. (Spec. 2.)

The Appellant's preemptive write back controller includes a list of the memory locations potentially requiring a write back (i.e., those that may have previously experienced a write operation) in a write back cache or other storage. The preemptive write back controller can initiate a preemptive cleaning of these locations. (*Id.* 4.)

B. ILLUSTRATIVE CLAIM

Claim 1, which further illustrates the invention, follows.

1. A preemptive write back system comprising:

a preemptive write back controller configured to initiate a memory system to perform a preemptive write back operation, wherein said preemptive write back controller includes:

a list for storing a plurality of pointers, each pointer representing a write back memory location candidate of said memory system, wherein said preemptive write back controller initiates said memory system to perform said preemptive write back operation by selecting one of said plurality of pointers of said list.

C. REJECTIONS

Claim 1 stands rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 6,119,205 ("Wicki").

Claims 1, 9-19, 41-45, 53-55, 57-61, 69-76, and 79-82 stand rejected under § 102(e) as anticipated by U.S. Patent No. 6,134,634 ("Marshall").

Claims 2-8, 46-52, 56, 62-68, 77, and 78 stand rejected under 35 U.S.C. § 103(a) as obvious over Marshall and U.S. Patent No. 5,434,993 ("Liencres").

II. ANTICIPATION BY WICKI

"Rather than reiterate the positions of parties *in toto*, we focus on the issue therebetween." *Ex parte Filatov*, No. 2006-1160, 2007 WL 1317144, at *2 (BPAI 2007). The Examiner finds, "Wicki clearly teaches . . . the speculative write back unit includes a list of tags (308, figure 4, read as pointers), each tag representing a write back memory location candidate of the memory (col. 8 lines 64-67) . . ." (Ans. 13.) The Appellant argues "that speculative write back unit 304 . . . is separate from tag store 308. This is very different from the structure of the preemptive write back controller of Claim 1, which includes a list of pointers to memory addresses that reside within the preemptive write back controller." (App. Br. 11.) Therefore, the issue is whether Wicki discloses a preemptive write back controller that stores pointers.

"Both anticipation under § 102 and obviousness under § 103 are two-step inquiries. The first step in both analyses is a proper construction of the claims The second step in the analyses requires a comparison of the properly construed claim to the prior art." *Medichem, S.A. v. Rolabo, S.L.*, 353 F.3d 928, 933, (Fed.Cir. 2003) (internal citations omitted).

A. CLAIM CONSTRUCTION

"[T]he PTO gives claims their 'broadest reasonable interpretation.'" *In re Bigio*, 381 F.3d 1320, 1324 (Fed. Cir. 2004) (quoting *In re Hyatt*, 211 F.3d 1367, 1372 (Fed. Cir. 2000)). "Moreover, limitations are not to be read into the claims from the specification." *In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993) (citing *In re Zletz*, 893 F.2d 319, 321 (Fed. Cir. 1989)).

Here, contrary to the Appellant's argument, claim 1 does not recite pointers to "memory addresses that reside within the preemptive write back controller." (App. Br. 11.) Instead, the claim recites in pertinent part the following limitations: "said preemptive write back controller includes: a list for storing a plurality of pointers, each pointer representing a write back memory location candidate of said memory system . . ." (*Id.*) Giving claim 1 the broadest, reasonable construction, the limitations require a preemptive write back controller that stores pointers.

B. ANTICIPATION ANALYSIS

"[A]nticipation is a question of fact." *In re Hyatt*, 211 F.3d 1367, 1371-72 (Fed. Cir. 2000) (citing *Bischoff v. Wethered*, 76 U.S. (9 Wall.)

812, 814-15 (1869); *In re Schreiber*, 128 F.3d 1473, 1477 (Fed. Cir. 1997)). "A reference anticipates a claim if it discloses the claimed invention 'such that a skilled artisan could take its teachings in *combination with his own knowledge of the particular art and be in possession of the invention.*'" *In re Graves*, 69 F.3d 1147, 1152 (Fed. Cir. 1995) (quoting *In re LeGrice*, 301 F.2d 929, 936 (CCPA 1962)). Of course, anticipation "is not an 'ipsissimis verbis' test." *In re Bond*, 910 F.2d 831, 832 (Fed. Cir. 1990) (citing *Akzo N.V. v. United States Int'l Trade Comm'n*, 808 F.2d 1471, 1479 n.11 (Fed. Cir. 1986)). "An anticipatory reference . . . need not duplicate word for word what is in the claims." *Standard Havens Prods. v. Gencor Indus.*, 953 F.2d 1360, 1369 (Fed. Cir. 1991).

Here, Wicki's "FIG. 3 illustrates in block diagram form a high level overview of a cache subsystem in accordance with the present invention; and FIG. 4 shows the cache subsystem . . . in greater detail . . ." (Col. 4, ll. 4-8.) For our part, we find that a subset of the cache subsystem, wherein the subset comprises the speculative write back unit 304 and the L2\$ tag store 308 show in the Figures, discloses the "preemptive write back controller" of claim 1. It is uncontested, moreover, that the L2\$ tag store 308 stores pointers. Because the subset of the cache subsystem includes the L2\$ tag store 308, and the L2\$ tag store 308 stores pointers, we agree with the Examiner that Wicki discloses a preemptive write back controller that stores pointers.

III. ANTICIPATION BY MARSHALL AND OBVIOUS OVER MARSHALL AND LIENCRES

The Examiner makes the following findings.

Marshall clearly teaches to initiate the memory system to perform a preemptive write back operation (col. 13 lines 50-52, i.e., process initiates a preemptive cache write back) by selecting one of a plurality of pointers of a list of pointers that resided in the write back controller (col. 13 lines 21-23, i.e., recalling cache tags for accessing cache entry)

(Ans. 15.) The Appellant argues, "Nowhere in the Marshall reference is initiating the memory system to perform a preemptive write back operation by selecting one of a plurality of pointers of a list of pointers that resides in the write back controller taught or suggested." (App. Br. 18.) Therefore, the issue is whether the Examiner has shown that Marshall initiates a preemptive write back by selecting one of a plurality of pointers.

A. CLAIM CONSTRUCTION

"The Patent and Trademark Office (PTO) must consider all claim limitations when determining patentability of an invention over the prior art." *In re Lowry*, 32 F.3d 1579, 1582 (Fed. Cir. 1994) (citing *In re Gulack*, 703 F.2d 1381, 1385 (Fed. Cir. 1983)).

Here, claim 1 recites in pertinent part the following limitations: "a plurality of pointers, each pointer representing a write back memory location candidate of said memory system, wherein said preemptive write back controller initiates said memory system to perform said preemptive write back operation by selecting one of said plurality of pointers of said

list." Claims 41 and 61 include similar limitations. Considering all the limitations, the three independent claims require initiating a preemptive write back by selecting one of a plurality of pointers wherein each pointer represents a location of a memory.

B. ANTICIPATION ANALYSIS

"[A]nticipation of a claim under § 102 can be found only if the prior art reference discloses every element of the claim . . ." *In re King*, 801 F.2d 1324, 1326 (Fed. Cir. 1986) (citing *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1458 (Fed. Cir. 1984)). "[A]bsence from the reference of any claimed element negates anticipation." *Kloster Speedsteel AB v. Crucible, Inc.*, 793 F.2d 1565, 1571 (Fed. Cir. 1986).

Here, Marshall's "FIG. 7 illustrates in flow chart form the process steps enabling a preemptive cache write-back . . ." (Col. 13, ll. 4-5.) The part of the reference cited by the Examiner explains that "Process **700** recalls the cache tags for the accessed cache entry (prossing [sic] block **704**)." *(Id. ll. 21-23.)* "These cache tags include write (WR) field **312**, nonwrite cycle (NWcycle) field **314**, read reclaim (RRclm) field **316** and dirty (D) field 318 illustrated in FIG. 3." *(Id. ll. 23-25.)*

The Examiner has not shown, however, that the recalled cache tags constitute pointers representing locations of a memory. To the contrary, Marshall explains that the "write field **312** preferably consists of a single

bit." (Col. 8, ll. 53-54.) "This write field **312** is reset to 0 upon first use of the cache entry. This field is set to 1 upon any write to the corresponding cache entry data." (*Id.* ll. 54-56.)

"The nonwrite cycle field **314** stores a write history of the corresponding cache entry." (*Id.* ll. 61-62.) "The read reclaim field **316** stores a read reclaim history of the corresponding cache entry." (*Id.* ll. 66-67.) "The dirty (D) field **318** is the conventional dirty field indicating whether the corresponding cache entry has been written to since the last write-back to main memory subsystem 105." (Col. 9, ll. 6-9.)

Because the Examiner has not shown that the recalled cache tags constitute pointers representing locations of a memory, he also has not shown that Marshall initiates a preemptive write back by selecting one of a plurality of pointers. The absence of initiating a preemptive write back by selecting one of a plurality of pointers negates anticipation.

C. OBVIOUSNESS ANALYSIS

The Examiner does not allege, let alone show, that the addition of Liencres cures the aforementioned deficiency of Marshall. Absent a teaching or suggestion of initiating a preemptive write back by selecting one of a plurality of pointers negates anticipation, we are unpersuaded of a *prima facie* case of obviousness.

IV. ORDER

For the aforementioned reasons, we affirm the rejection of claim 1 under § 102(b) as anticipated by Wicki. We reverse, however, the rejection of claims 1, 41, and 61 and of claims 9-19, 42-45, 53-55, 57-60, 69-76, and 79-82, which depend therefrom, as anticipated by Marshall. We also reverse the rejection of claims 2-8, 46-52, 56, 62-68, 77, and 78; which depend from claims 1, 41, and 61; as obvious over Marshall and Liencres.

"Any arguments or authorities not included in the brief or a reply brief filed pursuant to [37 C.F.R.] § 41.41 will be refused consideration by the Board, unless good cause is shown." 37 C.F.R. § 41.37(c)(1)(vii). Accordingly, our affirmance is based only on the arguments made in the Appeal Brief. Any arguments or authorities omitted therefrom are neither before us nor at issue but are considered waived. *Cf. In re Watts*, 354 F.3d 1362, 1367 (Fed. Cir. 2004) ("[I]t is important that the applicant challenging a decision not be permitted to raise arguments on appeal that were not presented to the Board.")

No time for taking any action connected with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN PART

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HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins CO 80527-2400