

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MANUEL JOSEPH ALVAREZ II, SANJAY RAGHUNATH DESHPANDE, KENNETH DOUGLAS KLAPPROTH, and DAVID MUI

Appeal 2007-3572
Application 10/162,636
Technology Center 2100

Decided: July 31, 2008

Before HOWARD B. BLANKENSHIP, ALLEN R. MACDONALD, and JAY P. LUCAS, *Administrative Patent Judges*.

BLANKENSHIP, *Administrative Patent Judge*.

DECISION ON APPEAL

This is an appeal under 35 U.S.C. § 134(a) from the Examiner's final rejection of claims 16-23, 25-32, 34-41, and 43-45, which are all the claims remaining in the application. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

Appellants' invention relates to a distributed system structure for a large-way, symmetric multiprocessor system using a bus-based cache-coherence protocol. A transaction tag format for a standard bus protocol is expanded to ensure unique transaction tags are maintained throughout the system. (Abstract.) Claim 16 is illustrative.

16. A method of managing transaction tags in a multiprocessor system, the transactions tags identifying transactions in the multiprocessing system, the method comprising the steps of:

receiving a transaction from a master device, wherein the transaction comprises a port-bus transaction tag, wherein the port-bus transaction tag comprises a source identifier that uniquely identifies the master device within a node that issued the transaction, and a transaction identifier that uniquely identifies the transaction in a set of transactions issued by the master device;

translating the port-bus transaction tag for the transaction to a system-level transaction tag; and

registering the transaction in an entry in a transaction registry, the transaction registry being a place for registering transactions.

The Examiner relies on the following references as evidence of unpatentability.

Newell	US 5,918,248	Jun. 29, 1999
Hagersten	US 6,351,795 B1	Feb. 26, 2002
Baker	US 6,594,735 B1	Jul. 15, 2003

(filed Dec. 28, 1998)

Claims 16-18, 23, 25-27, 32, 34-36, 41, and 43-45 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Baker.

Claims 19, 28, and 37 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Baker and Newell.

Claims 20-22, 29-31, and 38-40 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Baker, Newell, and Hagersten.

Baker

Baker describes a multi-processor, shared memory computing system 10 (Fig. 1). The system includes shared memory 12, processing elements (PE) 16, and input/output processors (IOP) 18. The shared memory 12 comprises memory modules 14. Baker col. 2, ll. 53-67. Each IOP 18 and PE 16 is connected with each shared memory module 14 by one of serial links 22 and 24, such that all data broadcast by a single IOP or PE is received by all the shared memory modules. Each shared memory module is further connected with each PE 16 and IOP 18 by a serial link 28. Each of the serial links 28 allows serial transfer of data from a shared memory module 14 to all IOPs 18 and PEs 16. *Id.*, col. 3, ll. 32-45.

Data is transferred between the PEs, IOPs, and shared memory modules in frames transferred on the links 22, 24, and 28. Each frame contains a three bit identifier, used to identify that frame as a request, response, or acknowledge frame. Groups of frames are used to complete transactions between modules 16, 18, and 14. Baker col. 3, ll. 46-55.

Each shared memory module 14 (Fig. 2) includes a tag memory 40 to store information identifying the present state of each group of thirty-two memory locations within main memory block 32. The data within tag memory 40 includes information concerning whether a group of memory locations is currently in use by a software task and, if so, the identifier of that task. If memory is “owned” it cannot be modified by other tasks executing on the system. Baker col. 3, l. 63 - col. 4, l. 31.

In a read transaction, for example, initiated by PE 16a (Fig. 1), processor system interface 60 (Fig. 3) generates a request frame consisting of a request type, a memory address, a sequence number, and a source identifier that identifies the originating PE 16a. The frame is transferred to PTC (pulse transmitter) 82 (Fig. 3) and broadcast to all shared modules 14. Baker col. 7, ll. 10-17.

Shared memory interfaces 36 of each memory module 14 (Fig. 3) uses a forty bit address space, while processors 52a and 52b of processing element 16 uses a thirty-two bit address space. Shared memory 12 (Fig. 1) may be split into two distinct address spaces -- one global shared forty bit address space, and thirty-two bit PE address sub-spaces. Mapping between PE address space and global shared memory address space is effected by processor system interface 60 of each PE 16. In particular, each processor system interface 60 includes an address mapper 70 (Fig. 7). Address mapper 70 maps the local thirty-two bit address space used by processor block 50 of a PE to a global forty bit address used by the memory modules 14. Baker col. 8, l. 63 - col. 9, l. 20.

Grouping of Claims

We will select a single representative claim from each of Appellants' argued groups. *See* 37 C.F.R. § 41.37(c)(1)(vii). Appellants do not provide separate arguments for the § 103(a) rejection of claims 19, 28, and 37 over Baker and Newell. Claims 19, 28, and 37 will thus stand or fall with respective base claims 18, 27, and 36 (of which 18 is representative). *See id.*

Claim 16 (25, 34)

The Examiner’s statement of the rejection of claim 16 is set forth at pages 3 and 4 of the Answer, in which the Examiner reads the claim recitations on elements in Baker. In particular, the Examiner finds that the “port-bus transaction tag” in Baker comprises the frame generated by a PE 16, which includes a source identifier for the originating PE and the request type (e.g., a “read” transaction). *See* Baker col. 7, ll. 10-17; col. 3, ll. 51-55.

Appellants advance numerous arguments in the Appeal Brief, to which we refer to the Examiner’s reasons in the Answer as to why the arguments are unavailing. Appellants’ position, as becomes apparent in the Reply Brief, is based on a narrow and unjustified reading of the terms of claim 16. The *claims* measure the invention. *See SRI Int’l v. Matsushita Elec. Corp.*, 775 F.2d 1107, 1121 (Fed. Cir. 1985) (en banc). Our reviewing court has repeatedly warned against confining the claims to specific embodiments described in the specification. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1323 (Fed. Cir. 2005) (en banc). During prosecution before the USPTO, claims are to be given their broadest reasonable interpretation, and the scope of a claim cannot be narrowed by reading disclosed limitations into the claim. *See In re Morris*, 127 F.3d 1048, 1054 (Fed. Cir. 1997); *In re Zletz*, 893 F.2d 319, 321 (Fed. Cir. 1989); *In re Prater*, 415 F.2d 1393, 1404-05 (CCPA 1969). “An essential purpose of patent examination is to fashion claims that are precise, clear, correct, and unambiguous. Only in this way can uncertainties of claim scope be removed, as much as possible, during the administrative process.” *In re Zletz*, 893 F.2d at 322.

Appellants acknowledge, at least, that a “destination address” is translated in Baker (Reply Br. 2), but then go on to allege there is no

translation of a “source identifier” and a “transaction identifier.” The claim that Appellants have submitted, however, does not require any translation of a source identifier; nor does it require any translation of a transaction identifier. The relevant step of claim 16 recites “translating the port-bus transaction tag for the transaction to a system-level transaction tag,” which is silent with respect to the particular elements that may be “translated” in the “tag.” Moreover, the claim recites that the tag “comprises,” or includes, a source identifier and a transaction identifier, but does not preclude other elements that make up the “tag.” Translating a destination address from a thirty-two bit processor-specific address to a forty-bit system-level address -- which even Appellants acknowledge that Baker describes -- is a comfortable fit within the meaning of translating a tag “for the transaction to a system-level transaction tag.”

Appellants also argue that tag memory 40 is “not described by Baker as being any type of transaction registry.” (Reply Br. 4.) For a prior art reference to anticipate in terms of 35 U.S.C. § 102, every element of the claimed invention must be identically shown in a single reference. However, this is not an “*ipsissimis verbis*” test. *In re Bond*, 910 F.2d 831, 832 (Fed. Cir. 1990). Appellants have alleged, but not demonstrated, error in the Examiner’s reasoning in the Answer with respect to why the information stored in tag memory 40 of Baker includes at least the minimal information recited in claim 16.

We have considered all of Appellants’ arguments in the briefs in support of claim 16, but are not persuaded of error in the Examiner’s finding of anticipation.

We also note that the Examiner, perhaps in an abundance of caution, has examined claim 16 as if all the terms are entitled to patentable weight. However, the claim recites receiving a “transaction” comprising a “tag” that comprises two “identifiers,” translating the “tag,” and registering (or storing) the “tag.” The information content of the “tag” -- i.e., what the tag may “identify” -- does not change the underlying structure or function of any machine or electronic memory, or serve to modify the actual requirements of the steps, of the invention set forth by claim 16. Appellants’ arguments based on the information content of what is received and stored thus rest on nonfunctional descriptive material. The *content* of nonfunctional descriptive material is not entitled to weight in the patentability analysis. *Cf. In re Lowry*, 32 F.3d 1579, 1583 (Fed. Cir. 1994) (“Lowry does not claim merely the information content of a memory. . . . Nor does he seek to patent the content of information resident in a database.”). *See also Ex parte Nehls* (BPAI Jan. 28, 2008), available at <http://www.uspto.gov/web/offices/dcom/bpai/prec/fd071823.pdf>; *Ex parte Curry*, 84 USPQ2d 1272 (BPAI 2005) (nonprecedential) (Fed. Cir. Appeal No. 2006-1003, *aff’d* Rule 36 Jun. 12, 2006); *Manual of Patent Examining Procedure* (MPEP) § 2106.01 (Eighth ed., Rev. 6, Sept. 2007).

We sustain the § 102 rejection of claim 16 over Baker.

Claim 17 (26, 35)

Appellants place claim 17 in a separate heading in the Appeal Brief. However, Appellants rely on the arguments, in regard to what Baker is alleged not to store in tag memory 40, that we have considered with respect to claim 16. Moreover, as we have indicated, the content of the information

(i.e., the “identifiers”) that are stored does not change the underlying structure or function of the memory, in the context of the invention of claim 17, and thus represents mere data, the content of which is not entitled to patentable weight. We sustain the § 102 rejection of claim 17.

Claim 18 (27, 36)

Appellants place claim 18 in a separate heading in the Appeal Brief. However, Appellants rely on the arguments, in regard to the composition of the frame described by Baker that we have considered with respect to claim 16. Moreover, the content of the system-level transaction tag -- the argued “identifiers” -- is not entitled to patentable weight in the invention set forth by claim 18. We sustain the § 102 rejection of claim 18.

Claim 43 (44, 45)

Appellants place claim 43 in a separate heading in the Appeal Brief. However, Appellants rely on the arguments, in regard to what Baker is alleged not to store in tag memory 40 that we have considered with respect to claim 16. Appellants also, apparently, read limitations into claim 43 that are not justified by the claim that is presented. While Appellants allege that a portion of Baker does not describe accessing memory using an index, instant claim 43 does not require that any memory be accessed using the index. In view of the “index” that is not used, the information content of the “tag” set forth by claim 43 is not entitled to patentable weight. We sustain the § 102 rejection of claim 43.

Claim 20 (29, 38)

The rejection of claim 20 under 35 U.S.C. § 103(a) as being unpatentable over Baker, Newell, and Hagersten is set forth at page 6 of the Answer.

Appellants' response to the rejection is that each of Baker and Hagersten teaches a "single level" of address translation, and there would have been no reason or motivation to modify a "single level" of address translation to the claim 20 "two-pronged address translation scheme." (App. Br. 15.) Appellants' reasoning consists of the allegation that a "single level of translation is all that is required to obtain the desired address mapping."
(Id.)

Appellants have not provided any evidence in support of the allegation. As the Examiner's rejection makes clear, the first and second translations are for different purposes that are described in Baker and Hagersten. Being not persuaded that a "single level of translation is all that is required," we are not persuaded of error in the Examiner's rejection of claim 20.

We sustain the § 103(a) rejection of claim 20.

Claim 21 (30, 39)

In response to the rejection of claim 21, Appellants allege (App. Br. 16) that the Examiner cites Baker's teachings at column 9, lines 20 through 45 as teaching "these claimed features." Actually, the Examiner has relied on the cited section of Baker only for the claim 21 first step of "receiving intervention data." Appellants have not provided an adequate response to

the rejection applied against claim 21. We are thus not persuaded of error in the rejection.

Moreover, claim 21 takes the form of receiving data, matching data with other data, and forwarding data. Nothing is done with the data other than the receiving, matching, and forwarding. The data in the context of claim 21 is mere data -- i.e., nonfunctional descriptive material -- the content of which is not entitled to patentable weight, for the reasons identified in our review of the rejection of claim 16.

We sustain the § 103(a) rejection of claim 21.

Claim 22 (31, 40)

In response to the rejection of claim 22, Appellants allege (App. Br. 16) that the cited portion of Newell does not describe any type of “tag matching,” including the “specifically recited step of matching a system transaction tag for a received (Rerun) command with a port-bus transaction tag for the received transaction.” We are not persuaded of error in the rejection of claim 22, at least for the reason that the Examiner does not allege that Newell by itself teaches “tag matching,” or the second step of instant claim 22. Nonobviousness cannot be established by attacking references individually where the rejection is based upon the teachings of a combination of references. *In re Merck & Co.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986) (citing *In re Keller*, 642 F.2d 413, 425 (CCPA 1981)).

Moreover, the nominal content of the data that is “matched” in the context of claim 22 is not entitled to patentable weight. Further, reissuing a tag “with an address modifier bit set” is no different from reissuing any “tag,” since the “address modifier bit” does nothing to affect the “reissuing.”

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Nor does claim 22 require that anything be done with the “address modifier bit,” or that the “bit” otherwise serves any function.

We sustain the § 103(a) rejection of claim 22.

CONCLUSION

As Appellants have not shown that any claim has been rejected in error, the rejection of claims 16-18, 23, 25-27, 32, 34-36, 41, and 43-45 under 35 U.S.C. § 102(e) and the rejection of claims 19-22, 28-31, and 37-40 under 35 U.S.C. § 103(a) are affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED

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